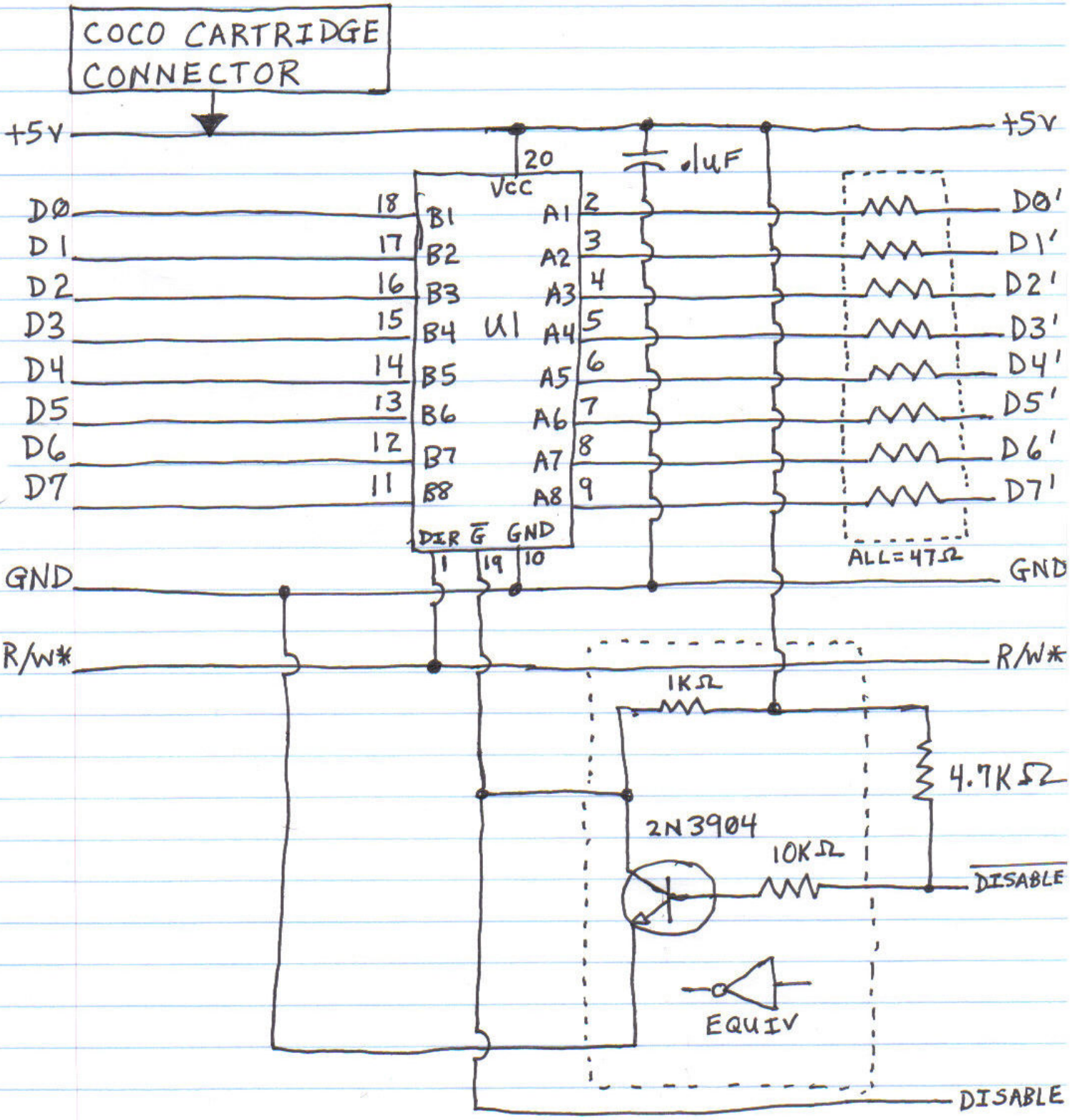
# BUFFERED "Y" CABLE FOR TRS-80 COLOR

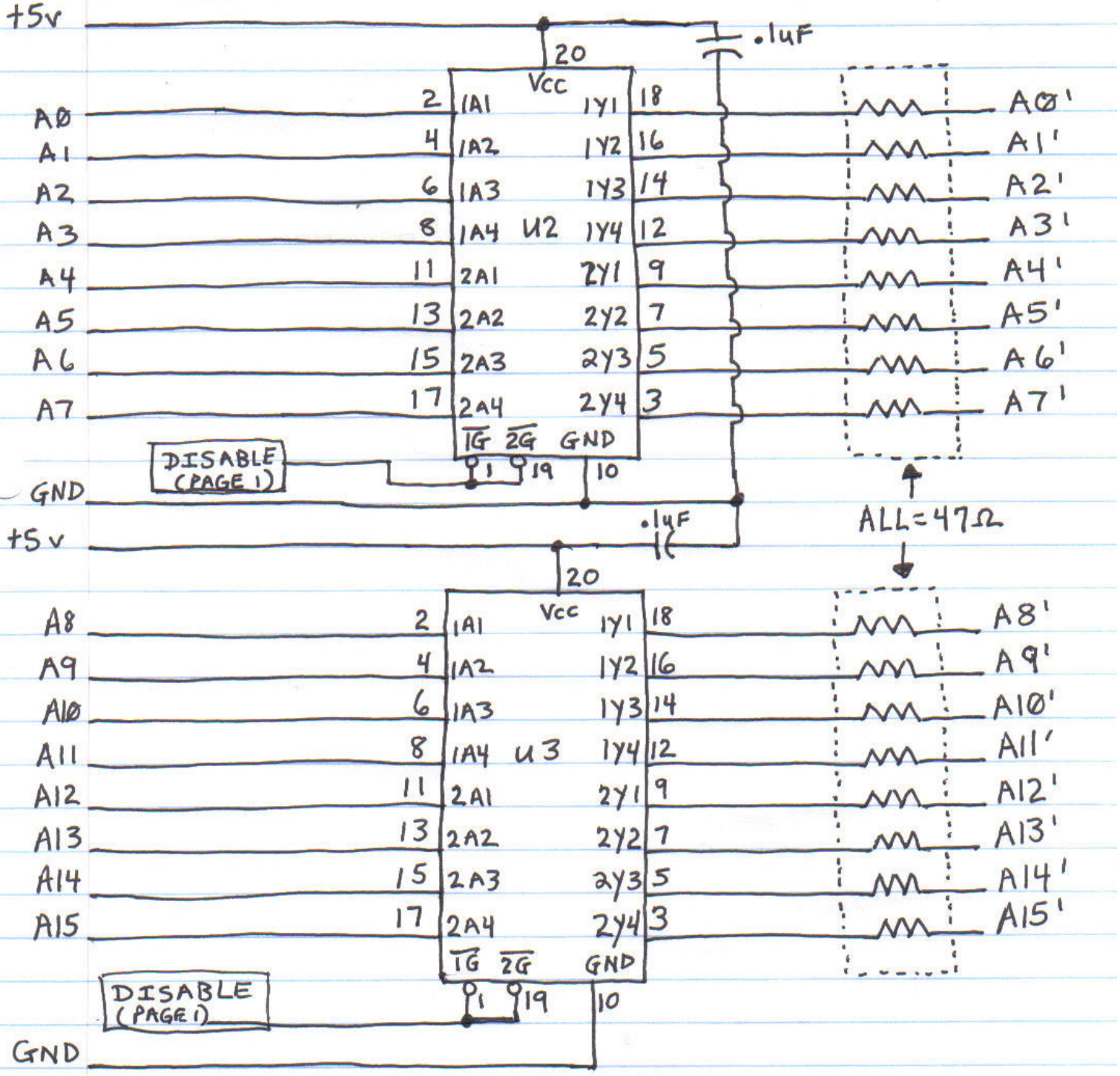
## DATA BUSS BUFFER



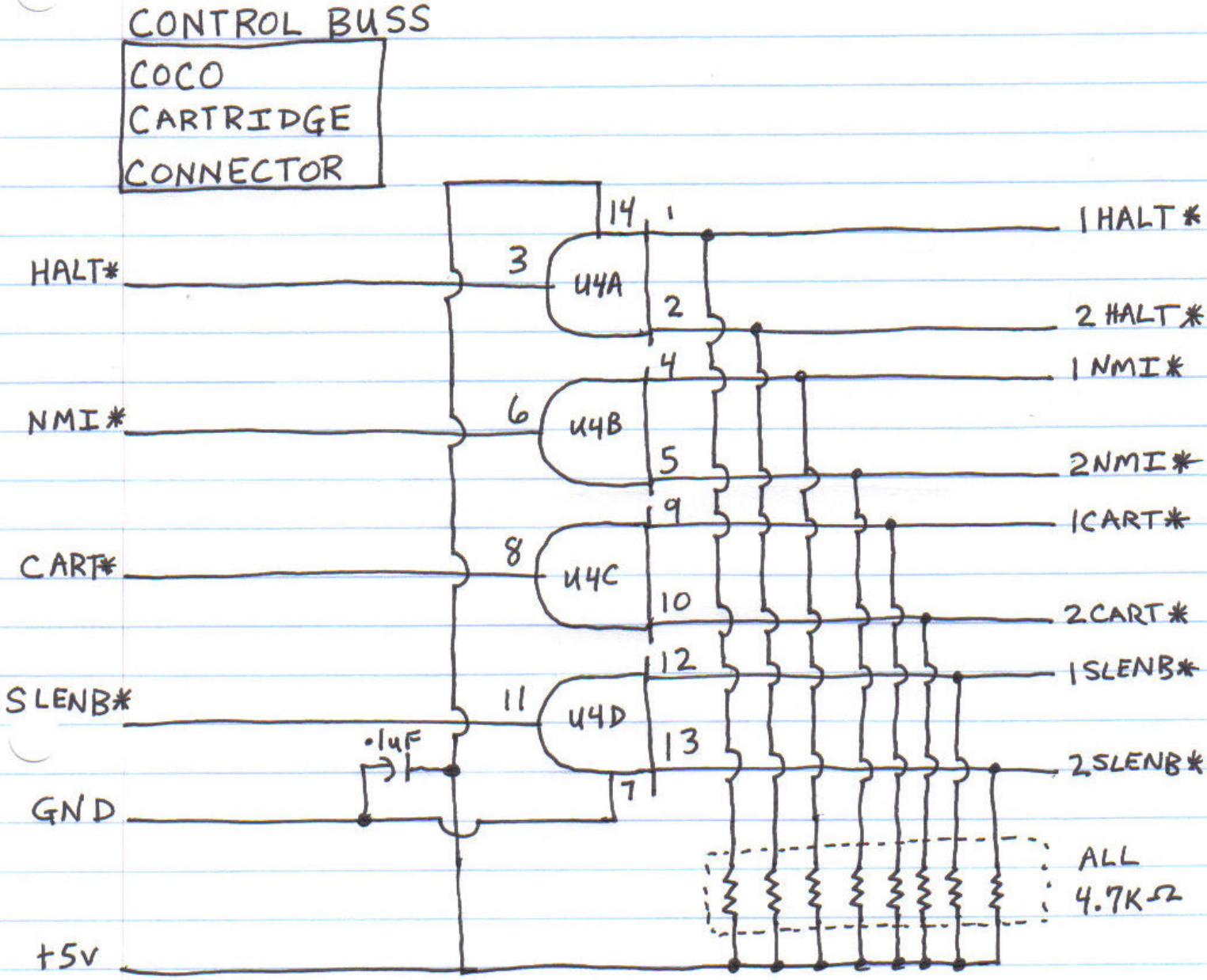

U1 = 74245 OPTIMAL "FAMILY" TO BE DETERMINED

# ADDRESS BUSS BUFFER

COCO CARTRIDGE CONNECTOR

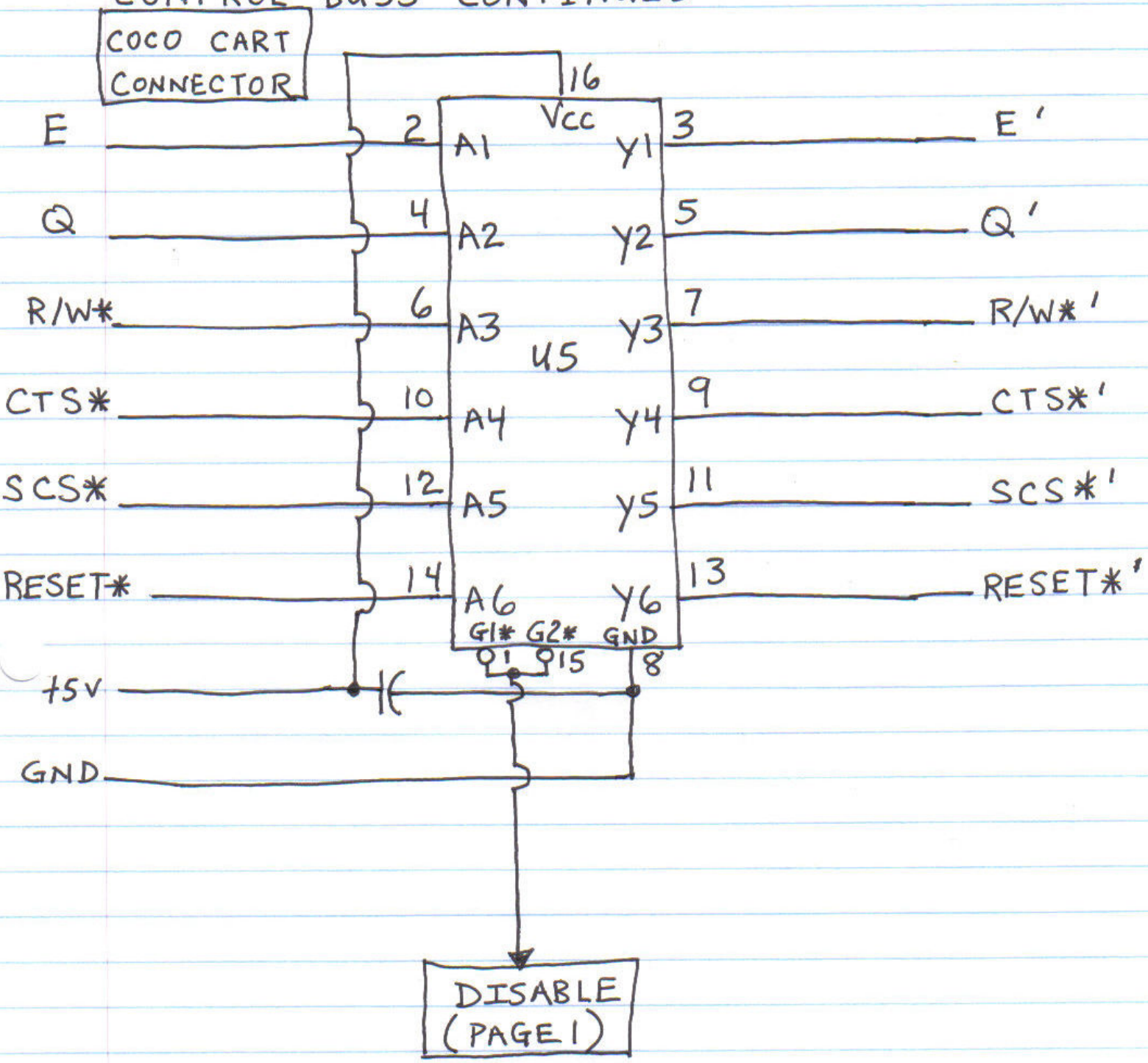



U2, U3 = 74244 OPTIMAL FAMILY T.B.D.



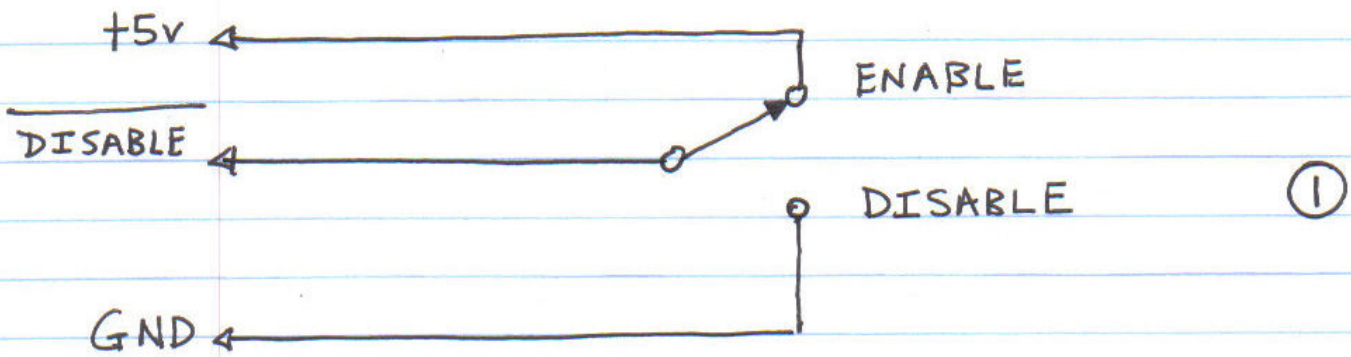

U4 = QUADRUPLE 2-INPUT POSITIVE-AND 7408
OPTIMAL FAMILY T.B.D.
(SCHMITT ANDS MAY BE PREFERABLE,
IF YOU CAN FIND THEM)

# CONTROL BUSS CONTINUED



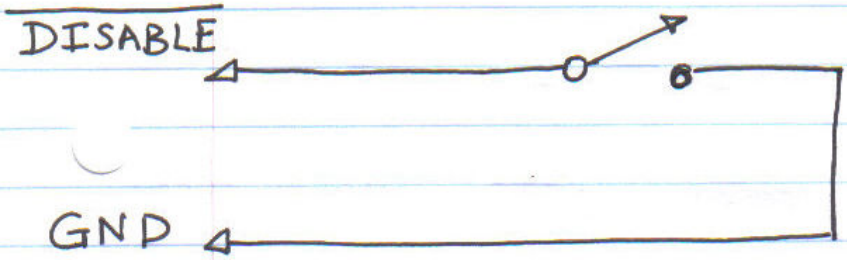

U5 = 74367 HEX-BUFFER
OPTIMAL FAMILY T.B.D.

DISABLE SWITCH




1

OR

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THE DISABLE SWITCH COMPLETELY DISCONNECTS THE BUFFERED "Y" CABLE AND ANY PERIPHERALS CONNECTED TO IT FROM THE BUSS.

IF USING METHOD #1 (S.P.D.T.) THEN THE 4.7KΩ RESISTOR ON PAGE 1 MAY BE OMITTED.

# OPTIONAL "MONITORING" CIRCUITRY

NOT IMPLEMENTED IN THE PROTOTYPE HOWEVER, TRANSISTOR BUFFERS DRIVING L.E.D.'S CAN BE USED TO MONITOR:

CTS* - USEFUL FOR "SEEING" WHEN THE CARTRIDGE ROM IS BEING ACCESSED.

SCS* - USEFUL FOR "SEEING" WHEN THE SCS* I/O AREA IS ACCESSED.

R/W* - USEFUL FOR "SEEING" A R/W* OPERATION.

RESET* - USEFUL FOR MONITORING SYSTEM RESET STATUS.

FOR R/W* AND POSSIBLY RESET*, I WOULD USE BI-POLAR (ANTI-PARALLEL) L.E.D.'S - RED/GREEN TO INDICATE DIFFERENT STATES. UNDER NORMAL OPERATION OF THE COMPUTER, THESE L.E.D.'S WOULD BE PRETTY MUCH USELESS, BUT DURING HARDWARE DEBUGGING, THEY MIGHT BE EXTREMELY USEFUL.

"PULSE-CATCHERS" COMPOSED OF $\overline{S/R}$ FLIP-FLOPS MIGHT BE EVEN MORE USEFUL.

ASSEMBLY

THE ENTIRE PROTOTYPE IS ASSEMBLED ON AN OLD VECTOR PLUG-BOARD THAT PLUGS INTO THE CARTRIDGE SLOT. THE "Y" IS COMPOSED OF TWO 40-PIN HEADERS. I HAVE USED UP TO 18" 40-WIRE RIBBON CABLE WITH A HEADER CONNECTOR CRIMPED TO ONE END AND A COCO-TYPE 40-PIN CARD CONNECTOR CRIMPED TO THE OTHER.

THIS DEVICE HAS BEEN EXPANDED TO A 16-SLOT MULTI-PAK COMPATIBLE INTERFACE WHICH INVOLVES THE CONSTRUCTION OF TWO 8-SLOT BOARDS. SEE PART TWO, BUT BE WARNED, THE CIRCUITRY GETS SOMEWHAT COMPLEX.