**WESTERN DIGITAL**
CORPORATION

# FD179X-02 Floppy Disk Formatter/Controller Family

**FEATURES**

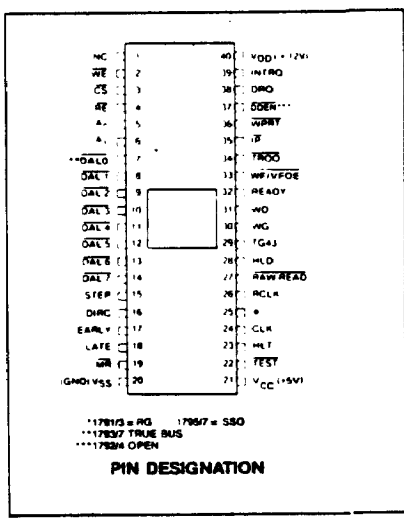
- TWO VFO CONTROL SIGNALS - RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY
- FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
  - Non IBM Format for Increased Capacity
- READ MODE
  Single/Multiple Sector Read with Automatic Search or Entire Track Read
  Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  Single/Multiple Sector Write with Automatic Sector Search
  Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  DMA or Programmed Data Transfers
  All Inputs and Outputs are TTL Compatible
  On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  Selectable Track to Track Stepping Time
  Side Select Compare
- INTERFACES TO WD1691 DATA SEPARATOR
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

**179X-02 FAMILY CHARACTERISTICS**

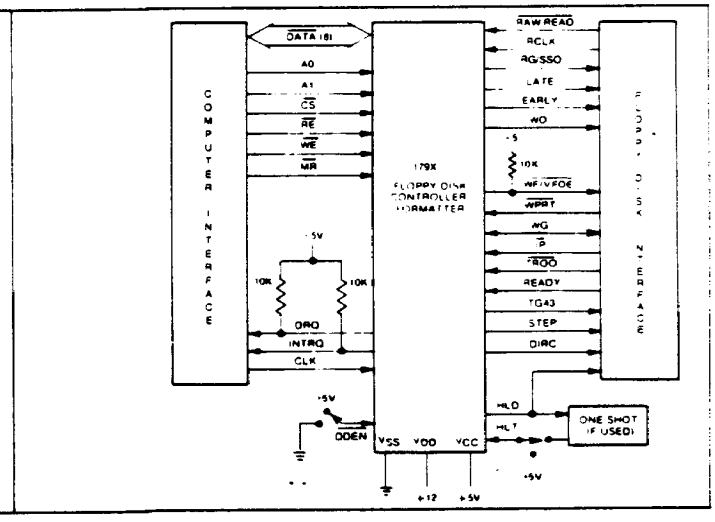
| FEATURES | 1791 | 1792 | 1793 | 1794 | 1795 | 1797 |
|---|---|---|---|---|---|---|
| Single Density (FM) | X | X | X | X | X | X |
| Double Density (MFM) | X | | X | | X | X |
| True Data Bus | | X | X | | X | |
| Inverted Data Bus | X | X | | X | | |
| Write Precomp | X | X | X | X | X | X |
| Side Selection Output | | | | X | X | |

**APPLICATIONS**

8" FLOPPY AND 5 1/4" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER




**PIN DESIGNATION**




**FD179X SYSTEM BLOCK DIAGRAM**



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**PIN OUTS**

| PIN NUMBER | PIN NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | NO CONNECTION | NC | Pin 1 is internally connected to a back bias generator and must be left open by the user. |
| 19 | MASTER RESET | $\overline{MR}$ | A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register. |
| 20 | POWER SUPPLIES | $V_{SS}$ | Ground |
| 21 | | $V_{CC}$ | +5V ±5% |
| 40 | | $V_{DD}$ | +12V ±5% |
| **COMPUTER INTERFACE:** | | | |
| 2 | WRITE ENABLE | $\overline{WE}$ | A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low. |
| 3 | CHIP SELECT | $\overline{CS}$ | A logic low on this input selects the chip and enables computer communication with the device. |
| 4 | READ ENABLE | $\overline{RE}$ | A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low. |
| 5,6 | REGISTER SELECT LINES | A0,A1 | These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:<br>$\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$<br>0 0 0 Status Reg Command Reg<br>0 0 1 Track Reg Track Reg<br>0 1 0 Sector Reg Sector Reg<br>0 1 1 Data Reg Data Reg |
| 7-14 | DATA ACCESS LINES | DAL0-DAL7 | Eight bit bi-directional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$. Each line will drive 1 standard TTL load. |
| 24 | CLOCK | CLK | This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ±1% for 8" drives, 1 MHz ±1% for mini-floppies. |
| 38 | DATA REQUEST | DRQ | This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5. |
| 39 | INTERRUPT REQUEST | INTRQ | This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5. |



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| PIN NUMBER | PIN NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| **FLOPPY DISK INTERFACE:** | | | |
| 15 | STEP | STEP | The step output contains a pulse for each step. |
| 16 | DIRECTION | DIRC | Direction Output is active high when stepping in, active low when stepping out. |
| 17 | EARLY | EARLY | Indicates that the WRITE DATA pulse occuring while Early is active (high) should be shifted early for write precompensation. |
| 18 | LATE | LATE | Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation. |
| 22 | $\overline{\text{TEST}}$ | $\overline{\text{TEST}}$ | This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers. |
| 23 | HEAD LOAD TIMING | HLT | When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD. |
| 25 | READ GATE (1791,1792,1793,1794) | RG | This output is used for synchronization of external data separators. The output goes high after two Bytes of zeroes in single density, or 4 Bytes of either zeroes or ones in double density operation. |
| 25 | SIDE SELECT OUTPUT (1794,1797) | SSO | The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector ID Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition. |
| 26 | READ CLOCK | RCLK | A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e., RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not. |
| 27 | $\overline{\text{RAW READ}}$ | $\overline{\text{RAW READ}}$ | The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition. |
| 28 | HEAD LOAD | HLD | The HLD output controls the loading of the Read-Write head against the media. |
| 29 | TRACK GREATER THAN 43 | TG43 | This output informs the drive that the Read / Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands. |
| 30 | WRITE GATE | WG | This output is made valid before writing is to be performed on the diskette. |
| 31 | WRITE DATA | WD | A 50ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats. |



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| PIN NUMBER | PIN NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 32 | READY | READY | This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7. |
| 33 | WRITE FAULT | WF/VFOE<br>VFO ENABLE | This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 function as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resister. |
| 34 | TRACK 00 | TR00 | This input informs the FD179X that the Read / Write head is positioned over Track 00. |
| 35 | INDEX PULSE | IP | This input informs the FD179X when the index hole is encountered on the diskette. |
| 36 | WRITE PROTECT | WPRT | This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit. |
| 37 | DOUBLE DENSITY | DDEN | This input pin selects either single or double density operation. When DDEN = 0, double density is selected. When DDEN = 1, single density is selected. This line must be left open on the 1792/4. |

## GENERAL DESCRIPTION

The FD179X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to Read/Write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bit directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793 respectively. On these devices, DDEN must be left open.

## ORGANIZATION

The Floppy Disk Formatter is illustrated in the block diagram. The primary sections include the parallel processor interface and the Floppy Disk Interface.

**Data Shift Register** - This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.



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**Data Register** - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

**Track Register** - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

**Sector Register (SR)** - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

**Command Register (CR)** - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

**Status Register (STR)** - This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

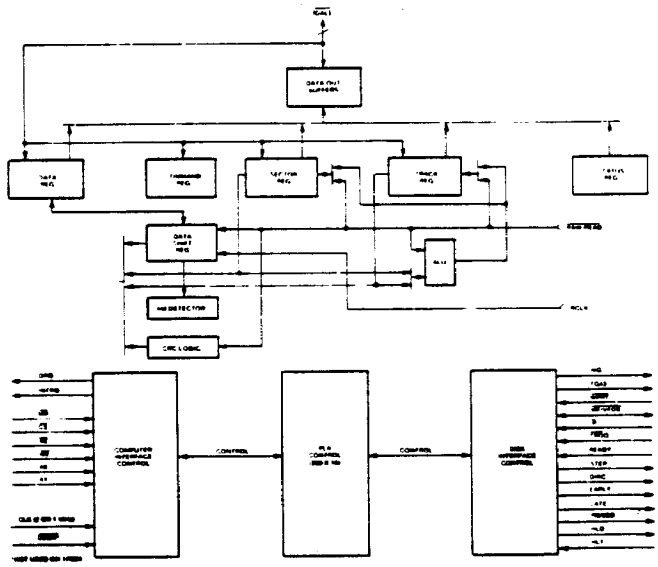
**CRC Logic** - This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^6 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

**Arithmetic/Logic Unit (ALU)** - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

**Timing and Control** - All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD179X has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN} = 0$ double density (MFM) is assumed. When $\overline{DDEN} = 1$, single density (FM) is assumed. 1792 & 1794 are single density only.



**FD179X BLOCK DIAGRAM**



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**AM Detector** - The address mark detector detects ID, data and Index address marks during read and write operations.

**PROCESSOR INTERFACE**

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

| A1 | A0 | READ ($\overline{RE}$) | WRITE ($\overline{WE}$) |
|---|---|---|---|
| 0 | 0 | Status Regiser | Command Register |
| 0 | 1 | Track Register | Track Register |
| 1 | 0 | Sector Register | Sector Register |
| 1 | 1 | Data Register | Data Register |

During Direct Memory Access (DMA) types of data transfers between the Data Register of the DF179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK Input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density.

**GENERAL DISK READ OPERATIONS**

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

| Sector Length Table* | |
|---|---|
| Sector Length Field (hex) | Number of Bytes in Sector (decimal) |
| 00 | 128 |
| 01 | 256 |
| 02 | 512 |
| 03 | 1024 |

*1795/97 may vary - see command summary.

The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations in 8" double density the FD179X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. THE RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1791/92/93/94 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when



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2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WFVFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

### GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read / Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault Input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault Input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM (DDEN = 1) and 200 ns pulses in MFM (DDEN = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD 179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

### READY

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

### COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

**TABLE 1. COMMAND SUMMARY**

A. Commands for Models: 1791, 1792, 1793, 1794

| | | Bits | | | | | | | | B. Commands for Models: 1795, 1797 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | Bits | | | | | | | |
| Type | Command | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I | Restore | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ |
| I | Seek | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ |
| I | Seek | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ | 0 | 0 | 1 | T | h | V | $r_1$ | $r_0$ |
| I | Step-in | 0 | 1 | 0 | T | h | V | $r_1$ | $r_0$ | 0 | 1 | 0 | T | h | V | $r_1$ | $r_0$ |
| I | Step-out | 0 | 1 | 1 | T | h | V | $r_1$ | $r_0$ | 0 | 1 | 1 | T | h | V | $r_1$ | $r_0$ |
| II | Read Sector | 1 | 0 | 0 | m | S | E | C | 0 | 1 | 0 | 0 | m | L | E | U | 0 |
| II | Write Sector | 1 | 0 | 1 | m | S | E | C | $a_0$ | 1 | 0 | 1 | m | L | E | U | $a_0$ |
| III | Read Address | 1 | 1 | 0 | 0 | 0 | E | 0 | 0 | 1 | 1 | 0 | 0 | 0 | E | U | 0 |
| III | Read Track | 1 | 1 | 1 | 0 | 0 | E | 0 | 0 | 1 | 1 | 1 | 0 | 0 | E | U | 0 |
| III | Write Track | 1 | 1 | 1 | 1 | 0 | E | 0 | 0 | 1 | 1 | 1 | 1 | 0 | E | U | 0 |
| IV | Force Interrupt | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ |



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**TABLE 2. FLAG SUMMARY**

**FLAG SUMMARY**

| Command Type | Bit No(s) | | Description |
|---|---|---|---|
| I | 0, 1 | $r_1r_0$ = Stepping Motor Rate<br>See Table 3 for Rate Summary | |
| I | 2 | V = Track Number Verify Flag | V = 0,No verify<br>V = 1,Verify on destination track |
| I | 3 | h = Head Load Flag | h = 1,Load head at beginning<br>h = 0 Unload head at beginning |
| I | 4 | T = Track Update Flag | T = 0,No update<br>T = 1,Update track register |
| II | 0 | $a_0$ = Data Address Mark | $a_0$ = 0,FB(DAM)<br>$a_0$ = 1,F8(deleted DAM) |
| II | 1 | C = Side Compare Flag | C = 0,Disable side compare<br>C = 1,Enable side compare |
| II & III | 1 | U = Update SSO | U = 0,Update SSO to 0<br>U = 1,Update SSO to 1 |
| II & III | 2 | E = 15 MS Delay | E = 0,No 15 MS delay<br>E = 1,15 MS delay |
| II | 3 | S = Side Compare Flag | S = 0,Compare for side 0<br>S = 1,Compare for side 1 |
| II | 3 | L = Sector Length Flag | LSB's Sector Length in ID Field<br>00: L=0 256, L=1 128<br>01: L=0 512, L=1 256<br>10: L=0 1024, L=1 512<br>11: L=0 128, L=1 1024 |
| II | 4 | m = Multiple Record Flag | m = 0,Single record<br>m = 1,Multiple records |
| IV | 0-3 | $I_x$ = Interrupt Condition Flags<br>$I_0$ = 1 Not Ready To Ready Transition<br>$I_1$ = 1 Ready To Not Ready Transition<br>$I_2$ = 1 Index Pulse<br>$I_3$ = 1 Immediate Interrupt, Requires A Reset<br>$I_3$-$I_0$ = 0 Terminate With No Interrupt (INTRQ) | |

NOTE: See Type IV Command Description for further information.



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## TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field ($r_0$ $r_1$), which determines the stepping motor rate as defined in Table 3.

A 2μs (MFM) or 4μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12μs before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

**TABLE 3. STEPPING RATES**

| CLK | 2 MHz | 2 MHz | 1 MHz | 1 MHz | 2 MHz | 1 MHz |
|---|---|---|---|---|---|---|
| $\overline{DDEN}$ | 0 | 1 | 0 | 1 | X | X |
| R1 R0 | $\overline{TEST}$ = 1 | $\overline{TEST}$ = 1 | $\overline{TEST}$ = 1 | $\overline{TEST}$ = 1 | $\overline{TEST}$ = 0 | $\overline{TEST}$ = 0 |
| 0 0 | 3 ms | 3 ms | 6 ms | 6 ms | 185μs | 368μs |
| 0 1 | 6 ms | 6 ms | 12 ms | 12 ms | 190μs | 380μs |
| 1 0 | 10 ms | 10 ms | 20 ms | 20 ms | 198μs | 396μs |
| 1 1 | 15 ms | 15 ms | 30 ms | 30 ms | 208μs | 416μs |

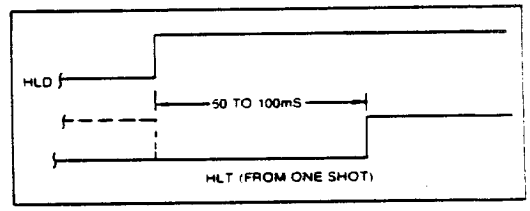
After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read / write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.




**HEAD LOAD TIMING**

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD 179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

**RESTORE (SEEK TRACK 0)**

Upon receipt of this comand the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the $r_1r_0$ field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state and that the DRQ pin stays low.



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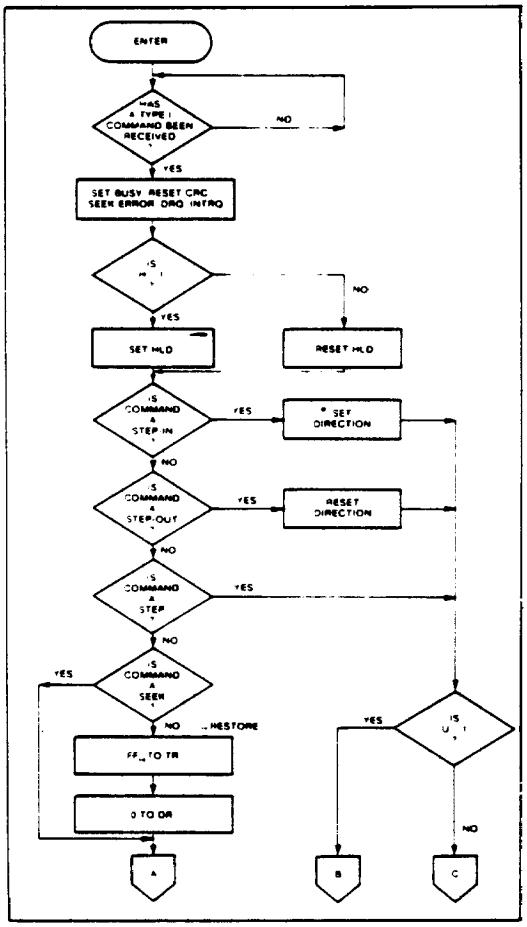
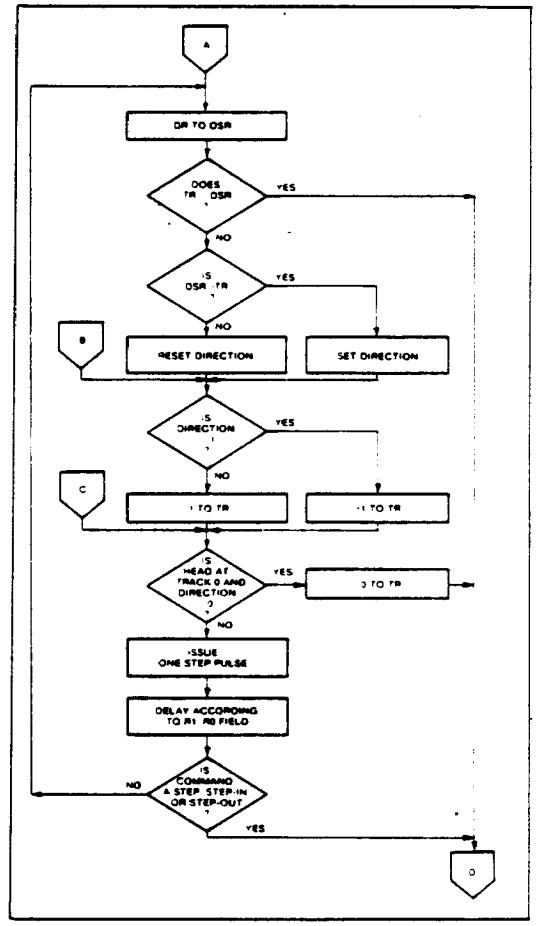



TYPE I COMMAND FLOW




TYPE I COMMAND FLOW

**SEEK**

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the register must be updated for the drive selected before seeks are issued.

**STEP**

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**STEP-IN**

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the



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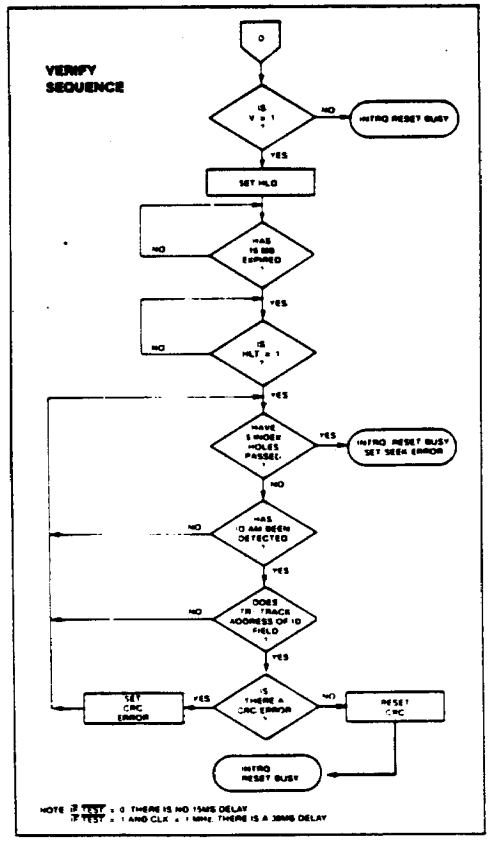
command. An interrupt is generated at the completion of the command.

**STEP-OUT**

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**EXCEPTIONS**

On the 1795 / 7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

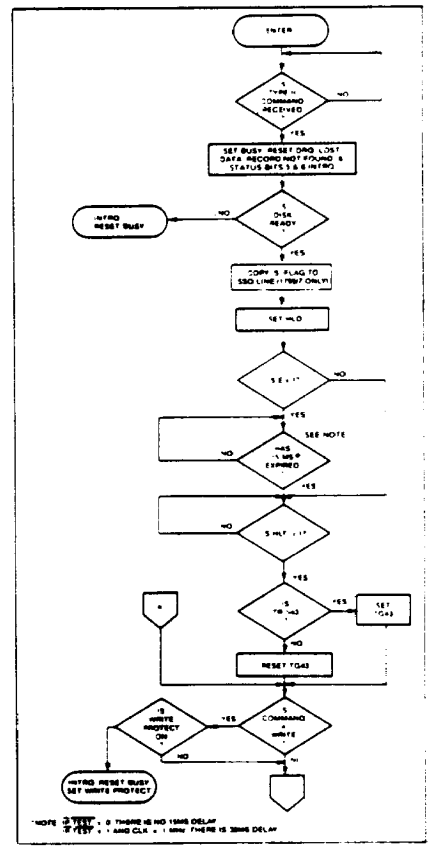



**TYPE I COMMAND FLOW**

**TYPE II COMMANDS**

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is ready and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record Not Found status bit is set (Status bit 3) and the command is terminated with an interrupt.



**TYPE II COMMAND**



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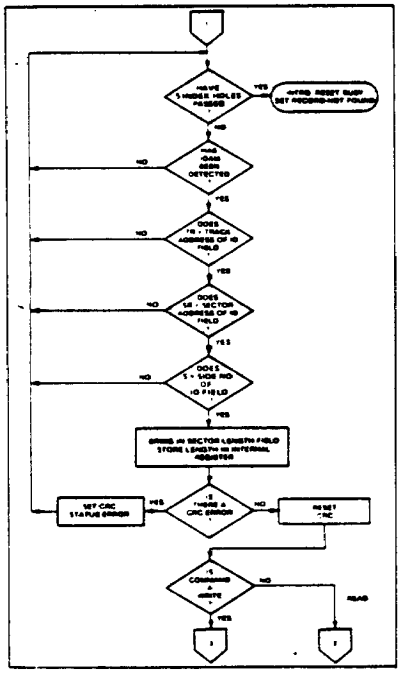
Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with sector register internally updated so that an address verification can occur on the next record. The WD179X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD 179X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD179X will search for 5 disk revolutions, interrupt out, reset busy, and set the Record Not Found status bit.

The Type II commands for 1791-94 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record Not Found status bit is set.



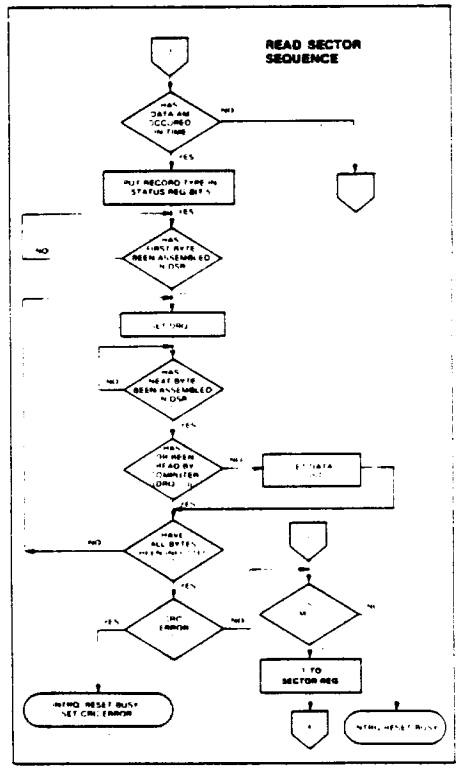
TYPE II COMMAND

The Type II and III commands contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 1795 / 7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'L' flag should be set to a one.

**READ SECTOR**

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID filed is searched for and verified again followed by the Data Address Mark search. If after 5 revolutions the DAM cannot be found, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the




TYPE II COMMAND



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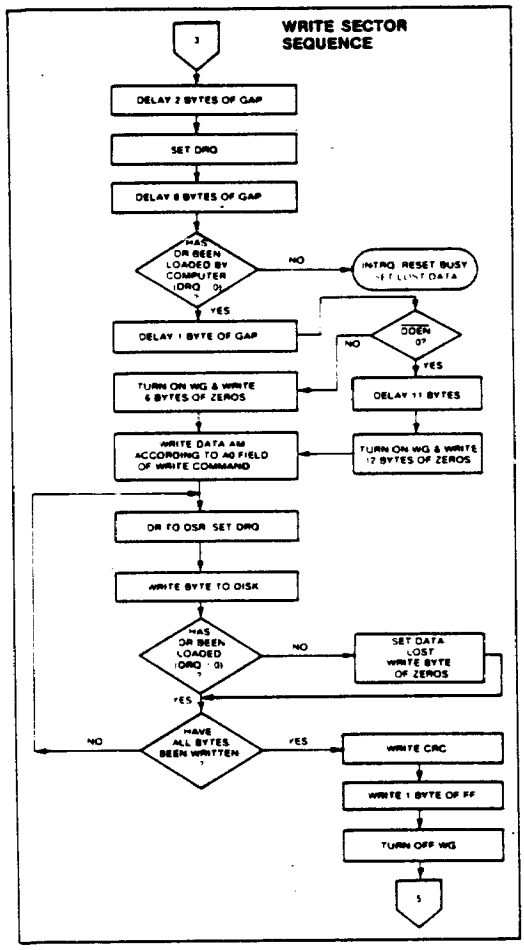


**TYPE II COMMAND**

data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

| STATUS BIT 5 | |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

**WRITE SECTOR**

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a0 field of the command as shown below:

| $a_0$ | Data Address Mark (Bit 0) |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Status Data Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12$\mu$sec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

**TYPE III COMMANDS**

**READ ADDRESS**

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

| TRACK ADDR | SIDE NUMBER | SECTOR ADDRESS | SECTOR LENGTH | CRC 1 | CRC 2 |
|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 |

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector



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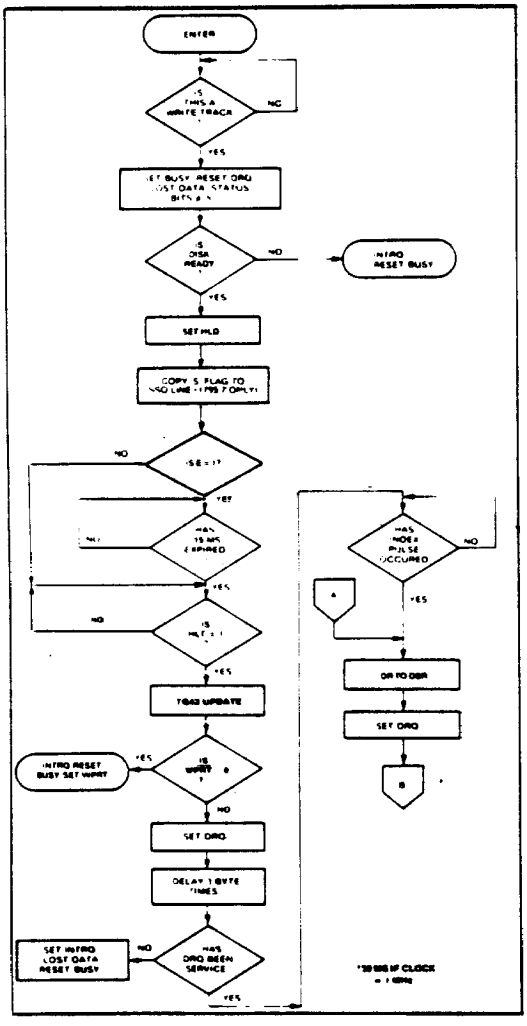
register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

### READ TRACK

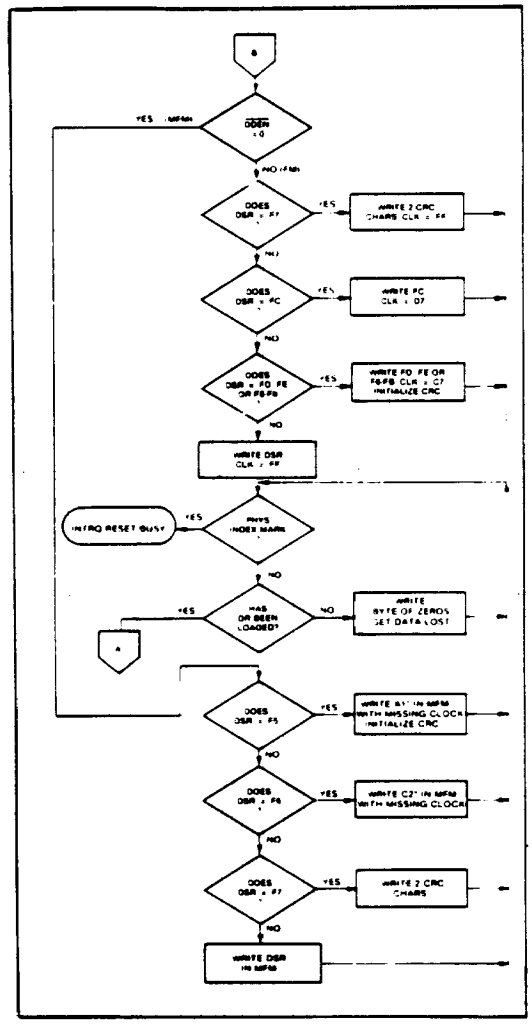
Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.




TYPE III COMMAND WRITE TRACK




TYPE III COMMAND WIRTE TRACK



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**CONTROL BYTES FOR INITIALIZATION**

| DATA PATTERN IN DR (HEX) | FD179X INTERPRETATION IN FM (DDEN = 1) | FD1791 / 3 INTERPRETATION IN MFM (DDEN = 0) |
|---|---|---|
| 00 thru F4 | Write 00 thru F4 with CLK = FF | Write 00 thru F4,in MFM |
| F5 | Not Allowed | Write A1* in MFM, Present CRC |
| F6 | Not Allowed | Write C2** in MFM |
| F7 | Generate 2 CRC bytes | Generate 2 CRC bytes |
| F8 thru FB | Write F8 thru FB, CLK = C7, Preset CRC | Write F8 thru FB, in MFM |
| FC | Write FC with CLK = D7 | Write FC in MFM |
| FD | Write FD with CLK = FF | Write FD in MFM |
| FE | Write FE, CLK = C7, Preset CRC | Write FE in MFM |
| FF | Write FF with CLK = FF | Write FF in MFM |

*Missing clock transition between bits 4 and 5. **Missing clock transition between bits 3 and 4.

**WRITE TRACK FORMATTING THE DISK**

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I / O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R / W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continued from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, of ID fields. Also, CRC's must be generated by an F7 pattern. Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

**TYPE IV COMMANDS**

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

$I_0$ = Not-Ready to Ready Transition
$I_1$ = Ready to Not-Read Transition
$I_2$ = Every Index Pulse
$I_3$ = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command ($I_3$-$I_0$) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If $I_3$-$I_0$ are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition ($I_3$ = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition ($I_1$ = 1) and the Every Index Pulse ($I_2$ = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.



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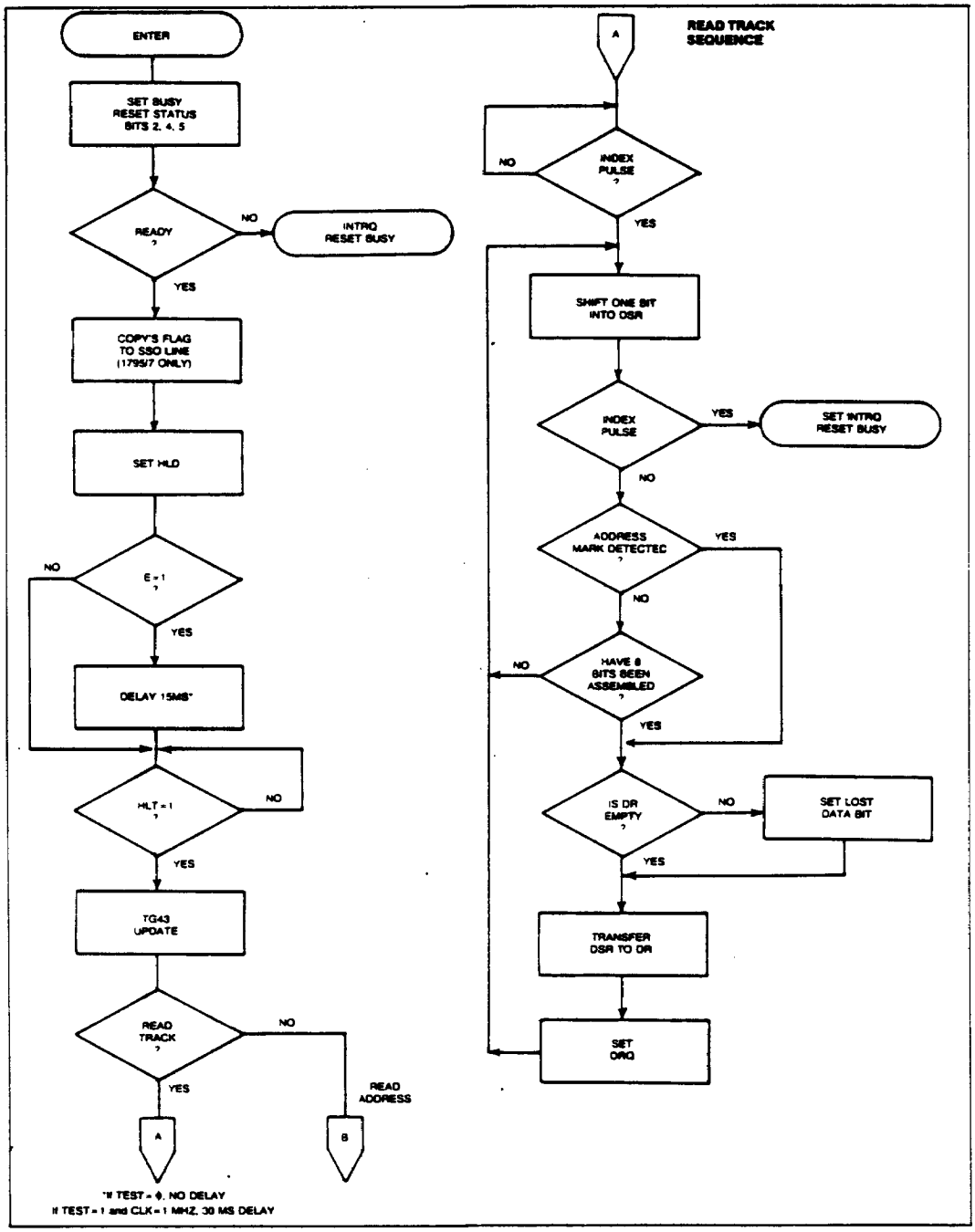


**TYPE III COMMAND**
Read Track / Address



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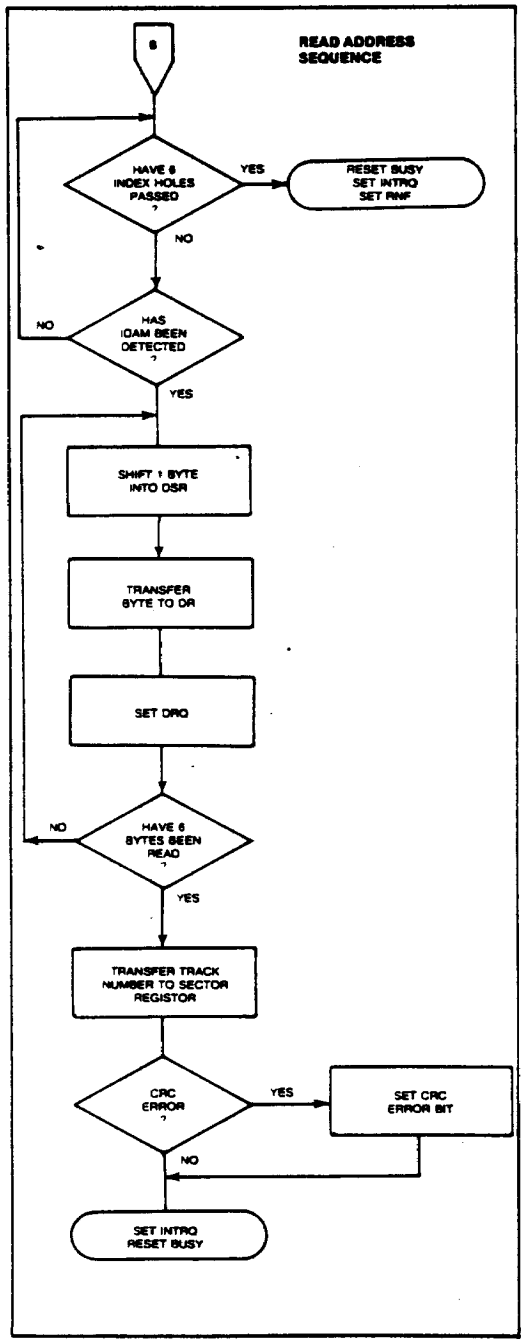


**TYPE III COMMAND**
Read Track / Address

## STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of that status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

| BITS | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I / O. They are: (times double when clock = 1 MHz)

| Operation | Next Operation | Delay Req'd. FM | MFM |
|---|---|---|---|
| Write to Command Reg. | Read Busy Bit (Status Bit 0) | 12$\mu$s | 6$\mu$s |
| Write to Command Reg. | Read Status Bits 1-7 | 28$\mu$s | 14$\mu$s |
| Write Any Register | Read From Diff. Register | 0 | 0 |

### IBM 3740 FORMAT - 128 BYTES / SECTOR

Shown below is the IBM single-density format with 128 bytes / sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.



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### IBM 3740 FORMAT - 128 BYTES / SECTOR

Shown below is the IBM single-density format with 128 bytes / sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

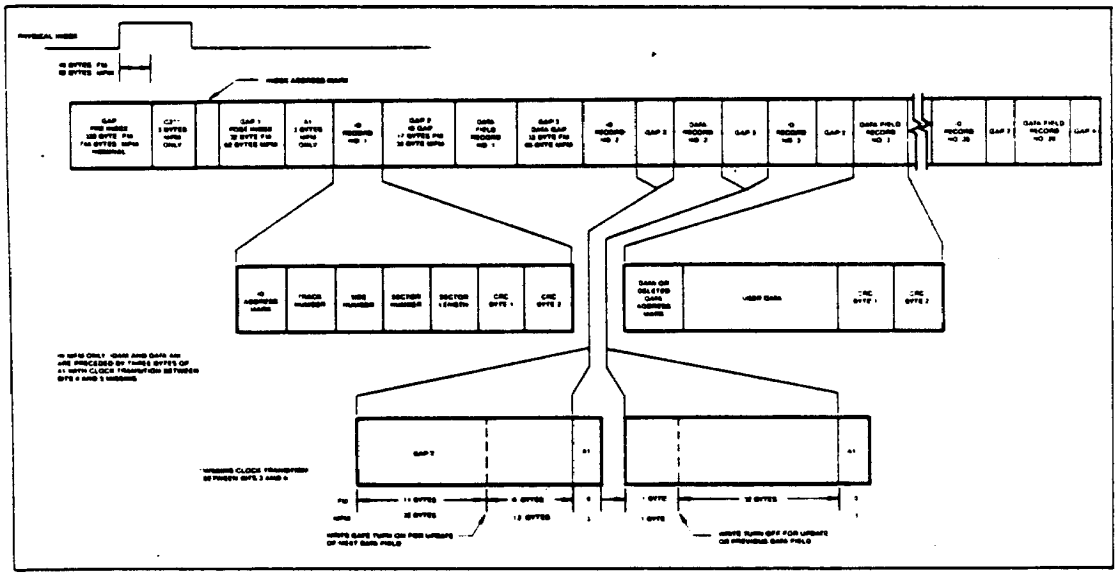
| | NUMBER OF BYTES | HEX VALUE OF BYTE WRITTEN |
|---|---|---|
| | 40 | FF (or 00)[1] |
| | 6 | 00 |
| | 1 | FC (Index Mark) |
| * | 26 | FF (or 00)[1] |
| | 6 | 00 |
| | 1 | FE (ID Address Mark) |
| | 1 | Track Number |
| | 1 | Side Number (00 or 01) |
| | 1 | Sector Number (1 thru 1A) |
| | 1 | 00 (Sector Length) |
| | 1 | F7 (2 CRC's written) |
| | 11 | FF (or 00)ses E5)[1] |
| | 6 | 00 |
| | 1 | FB (Data Address Mark) |
| | 128 | Data (IBM uses E5) |
| | 1 | F7 (2 CRC's written) |
| | 27 | FF (or 00)[1] |
| | 247** | FF (or 00)[1] |

*Write bracketed field 26 times.
**Continue writing until FD179X interrupts out. Approx. 247 bytes.
1-Optional '00' on 1795/7 only.

Shown below is the IBM dual-density format with 256 bytes / sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

| | NUMBER OF BYTES | HEX VALUE OF BYTE WRITTEN |
|---|---|---|
| | 80 | 4E |
| | 12 | 00 |
| | 3 | F6 (Writes C2) |
| | 1 | FC (Index Mark) |
| * | 50 | 4E |
| | 12 | 00 |
| | 3 | F5 (Writes A1) |
| | 1 | FE (ID Address Mark) |
| | 1 | Track Number (0 thru 4C) |
| | 1 | Side Number (0 or 1) |
| | 1 | Sector Number (1 thru 1A) |
| | 1 | 01 (Sector Length) |
| | 1 | F7 (2 CRC's written) |
| | 22 | 4E |
| | 12 | 00 |
| | 3 | F5 (Writes A1) |
| | 1 | FB (Data Address Mark) |
| | 256 | DATA |
| | 1 | F7 (2 CRC's written) |
| | 54 | 4E |
| | 598** | 4E |

*Write bracketed field 26 times.
**Continue writing until FD179X interrupts out. Approx. 598 bytes.



IBM TRACK FORMAT



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## 1. NON-IBM FORMATS

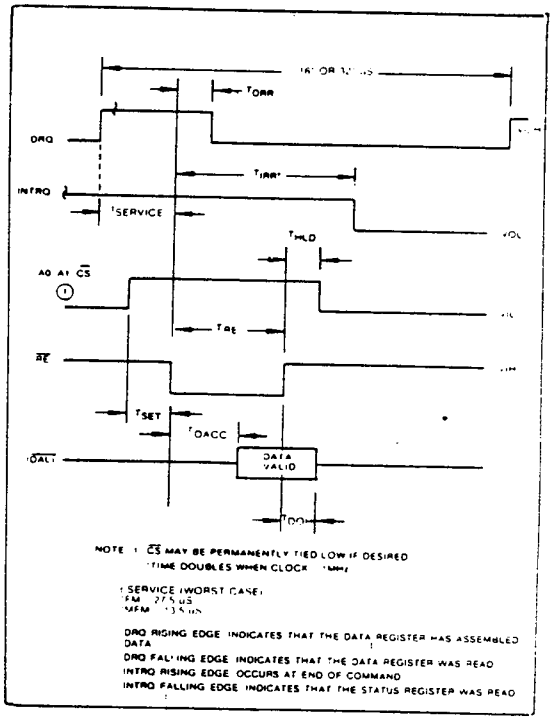
Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512, 1024 bytes.
2) Gap 2 cannot be vaired from the IBM format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD179X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

| | FM | MFM |
|---|---|---|
| Gap I | 16 bytes FF | 32 bytes 4E |
| Gap II | 11 bytes FF | 22 bytes 4E |
| * | 6 bytes 00 | 12 bytes 00 |
| * | | 3 bytes A1 |
| Gap III** | 10 bytes FF | 24 bytes 4E |
| | 4 bytes 00 | 8 bytes 00 |
| | | 3 bytes A1 |
| Gap IV | 16 bytes FF | 16 bytes 4E |

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.




READ ENABLE TIMING

### TIMING CHARACTERISTICS

$T_A$ = 0°C to 70°C, $V_{DD}$ = +12V ± .6V, $V_{SS}$ = 0V, $V_{CC}$ = +5V ± .25V

**READ ENABLE TIMING**

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| TSET | Setup ADDR & CS to $\overline{RE}$ | 50 | | | nsec | |
| THLD | Hold ADDR & CS from $\overline{RE}$ | 10 | | | nsec | |
| TRE | $\overline{RE}$ Pulse Width | 400 | | | nsec | $C_L$ = 50 pf |
| TDRR | DRQ Reset from $\overline{RE}$ | | 400 | 500 | nsec | |
| TIRR | INTRQ Reset from $\overline{RE}$ | | 500 | 3000 | nsec | See Note 5 |
| TDACC | Data Access from $\overline{RE}$ | | | 350 | nsec | $C_L$ = 50 pf |
| TDOH | Data Hold From $\overline{RE}$ | 50 | | 150 | nsec | $C_L$ = 50 pf |

**WRITE ENABLE TIMING** (See Note 6, Page 21)

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| TSET | Setup ADDRS & CS TO $\overline{WE}$ | 50 | | | nsec | |
| THLD | Hold ADDR & CS from $\overline{WE}$ | 10 | | | nsec | |
| TWE | $\overline{WE}$ Pulse Width | 350 | | | nsec | |
| TDRR | DRQ Reset from $\overline{WE}$ | | 400 | 500 | nsec | |
| TIRR | INTRQ Reset from $\overline{WE}$ | | 500 | 3000 | nsec | See Note 5 |
| TDS | Data Setup to $\overline{WE}$ | 250 | | | nsec | |
| TDH | Data Hold from $\overline{WE}$ | | 70 | | nsec | |



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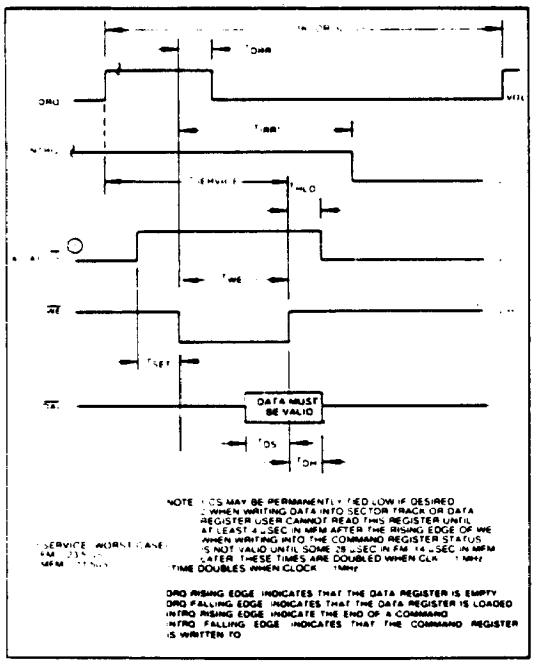
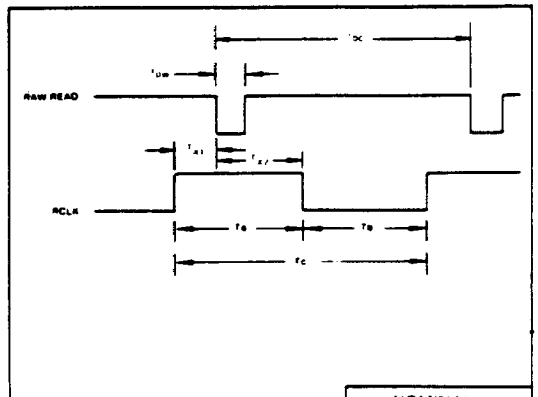



**WRITE ENABLE TIMING**




| DISKETTE | MODE | $\overline{DDEN}$ | CLK | NOMINAL $T_a$ | NOMINAL $T_b$ | NOMINAL $T_c$ |
|---|---|---|---|---|---|---|
| 8" | MFM | 0 | 2 MHz | 1 µs | 1 µs | 2 µs |
| 8" | FM | 1 | 2 MHz | 2 µs | 2µs | 4 µs |
| 5" | MFM | 0 | 1 MHz | 2 µs | 2µs | 4 µs |
| 5" | FM | 1 | 1 MHz | 4 µs | 4 µs | 8 µs |

**INPUT DATA TIMING**

**INPUT DATA TIMING:**

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| $T_{PW}$ | $\overline{\text{Raw Read}}$ Pulse Width | 100 | 200 | | nsec | See Note 1 |
| $T_{BC}$ | Raw Read Cycle Time | 1500 | 2000 | | nsec | 1800 ns @ 70°C |
| $T_{CK}$ | RCLK Cycle Time | 1500 | 2000 | | nsec | 1800 ns @ 70°C |
| $T_{X1}$ | RCLK hold to $\overline{\text{Raw Read}}$ | 40 | | | nsec | See Note 1 |
| $T_{X2}$ | $\overline{\text{Raw Read}}$ hold to RCLK | 40 | | | nsec | See Note 1 |

**WRITE DATA TIMING:(ALL TIMES DOUBLE WHEN CLK = 1 MHz)**

| SYMBOL | CHARACTERISTICS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| Twp | Write Data Pulse Width | | 500 | 650 | nsec | FM |
| | | | 200 | 350 | nsec | MFM |
| Twg | Write Gate to Write DATA | | 2 | | µsec | FM |
| | | | 1 | | µsec | MFM |
| Tbc | Write Data Cycle Time | | 2,3,or 4 | | µsec | ± CLK Error |
| Ts | Early (Late) to Write Data | 125 | | | nsec | MFM |
| Th | Early (Late) From Write Data | 125 | | | nsec | MFM |
| Twf | Write Gate off from WD | | 2 | | µsec | FM |
| | | | 1 | | µsec | MFM |
| Twdl | WD Valid Clk | 100 | | | nsec | CLK = 1 MHz |
| | | 50 | | | nsec | CLK = 2 MHz |
| Twd2 | WD Valid after CLK | 100 | | | nsec | CLK = 1 MHZ |
| | | 30 | | | nsec | CLK = 2 MHz |



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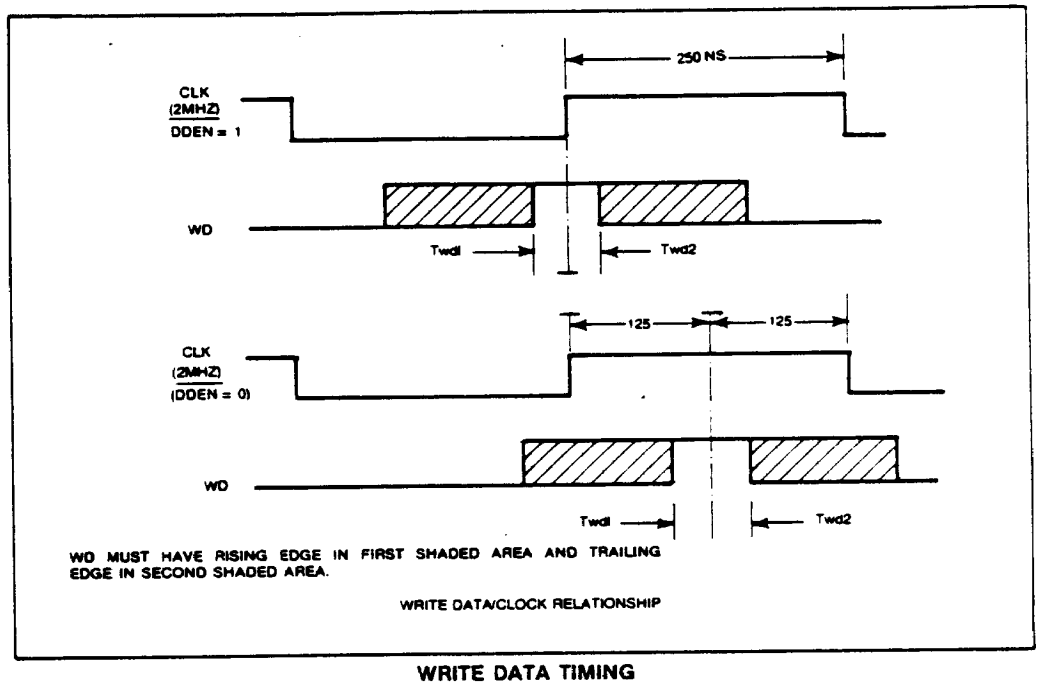


**WRITE DATA TIMING**

**MISCELLANEOUS TIMING: (Times Double When Clock = 1MHz)**

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| $TCD_1$ | Clock Duty (low) | 230 | 250 | 20000 | nsec | |
| $TCD_2$ | Clock Duty (high) | 200 | 250 | 20000 | nsec | |
| TSTP | Step Pulse Output | 2 or 4 | | | µsec | See Note 5 |
| TDIR | Dir Setup to Step | | 12 | | µsec | ± CLK ERROR |
| TMR | Master Reset Pulse Width | 50 | | | µsec | |
| TIP | Index Pulse Width | 10 | | | µsec | See Note 5 |
| TWF | Write Fault Pulse Width | 10 | | | µsec | |



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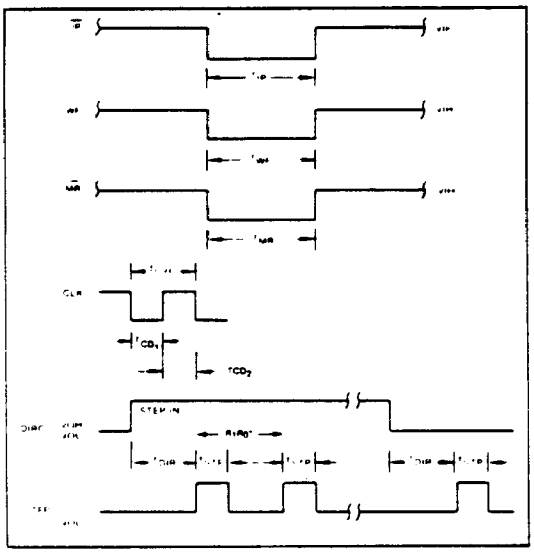

**MISCELLANEOUS TIMING**

*FROM STEP RATE TABLE

**NOTES:**

1. Pulse width on $\overline{\text{RAW READ}}$ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2$\mu$s, nominal in MFM and 4$\mu$s nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).
5. Times double when clock = 1 MHz.
6. Output timing readings are at $V_{OL}$ = 0.8v and $V_{OH}$ = 2.0v.

**Table 4. STATUS REGISTER SUMMARY**

| BIT | ALL TYPE I COMMANDS | READ ADDRESS | READ SECTOR | READ TRACK | WRITE SECTOR | WRITE TRACK |
|---|---|---|---|---|---|---|
| S7 | NOT READY | NOT READY | NOT READY | NOT READY | NOT READY | NOT READY |
| S6 | WRITE PROTECT | 0 | 0 | 0 | WRITE PROTECT | WRITE PROTECT |
| S5 | HEAD LOADED | 0 | RECORD TYPE | 0 | WRITE FAULT | WRITE FAULT |
| S4 | SEEK ERROR | RNF | RNF | 0 | RNF | 0 |
| S3 | CRC ERROR | CRC ERROR | CRC ERROR | 0 | CRC ERROR | 0 |
| S2 | TRACK 0 | LOST DATA | LOST DATA | LOST DATA | LOST DATA | LOST DATA |
| S1 | INDEX PULSE | DRQ | DRQ | DRQ | DRQ | DRQ |
| S0 | BUSY | BUSY | BUSY | BUSY | BUSY | BUSY |

**STATUS FOR TYPE I COMMANDS**

| BIT NAME | MEANING |
|---|---|
| S7 NOT READY | This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ored" with MR. |
| S6 PROTECTED | When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input. |
| S5 HEAD LOADED | When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals. |
| S4 SEEK ERROR | When set, the desired track was not verified. This bit is reset to 0 when updated. |
| S3 CRC ERROR | CRC encountered in ID field. |
| S2 TRACK 00 | When set, indicates Read / Write head is positioned to Track 0. This bit is an inverted copy of the TR00 input. |
| S1 INDEX | When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input. |
| S0 BUSY | When set, command is in progress. When reset no command is in progress. |



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**STATUS FOR TYPE II AND III COMMANDS**

| BIT NAME | MEANING |
|---|---|
| S7 NOT READY | This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ORed" with MR. The Type II and III Commands will not execute unless the drive is ready. |
| S6 WRITE PROTECT | On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated. |
| S5 RECORD TYPE WRITE FAULT | On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated. |
| S4 RECORD NOT FOUND (RNF) | When set, it indicates that the desire track, sector, or side were not found. This bit is reset when updated. |
| S3 CRC ERROR | If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated. |
| S2 LOST DATA | When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. |
| S1 DATA REQUEST | This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. |
| S0 BUSY | When set, command is under execution. When reset, no command is under execution. |

**ELECTRICAL CHARACTERISTICS**

Absolute Maximum Ratings

$V_{DD}$ with respect to $V_{SS}$(ground): +15 to -0.3V
Voltage to any input with respect to $V_{SS}$ = +15 to -0.3V
$I_{CC}$ = 60 MA (35 MA nominal)
$I_{DD}$ = 15 MA (10 MA nominal)

$C_{IN}$ & $C_{OUT}$ = 15 pF max with all pins grounded except one under test.
Operating temperature = 0°C to 70°C
Storate temperature = -55°C to +125°C

**OPERATING CHARACTERISTICS (DC)**

TA = 0°C to 70°C, $V_{DD}$ = +12V ± .6V, $V_{SS}$ = OV, $V_{CC}$ = +5V ± .25V

| SYMBOL | CHARACTERISTIC | MIN. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage | | 10 | μA | $V_{IN}$ = $V_{DD}$** |
| $I_{OL}$ | Output Leakage | | 10 | μA | $V_{OUT}$ = $V_{DD}$ |
| $V_{IH}$ | Input High Voltage | 2.6 | | V | |
| $V_{IL}$ | Input Low Voltage | | 0.8 | V | |
| $V_{OH}$ | Output High Voltage | 2.8 | | V | $I_0$ = -100μA |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_0$ = 1.6mA |
| $P_D$ | Power Dissipation | | 0.6 | W | |

*1792 and 1794 $I_0$ = 1.0 mA
**Leakage conditions are for input pins without internal pull-up resistors. Pins 22, 23, 33, 36, and 37 have pull-up resistors.



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# FD179X Application Notes

## INTRODUCTION

Over the past several years, the Floppy Disk Drive has become the most popular on-line storage device for mini and microcomputer systems. Its fast access time, reliability and low cost-per-bit ratio enables the Floppy Disk Drive to be the solution in mass storage for microprocessor systems. The drive interface to the Host system is standardized, allowing the OEM to substitute one drive for another with minimum hardware/software modifications.

Since Floppy Disk Data is stored and retrieved as a self-clocking serial data stream, some means of separating the clock from the data and assembling this data in parallel form must be accomplished. Data is stored on individual Tracks of the media, requiring control of a stepper motor to move the Read/Write head to a predetermined Track. Byte synchronization must also be accomplished to ensure that the parallel data is properly assembled. After all the design considerations are met, the final controller can consist of 40 or more TTL packages.

To alleviate the burden of Floppy Disk Controller design, Western Digital has developed a Family of LSI Floppy Disk controller devices. Through its own set of macro commands, the FD179X Controller Family will perform all the functions necessary to read and write data to the drive. Both the 8" standard and 5 ¼" mini-floppy are supported with single or double density recording techniques. The FD179X is compatible with the IBM 3740 (FM) data format, or the System 34 (MFM) standards. Provisions for non-standard formats and variable sector lengths have been included to provide more storage capability per track. Requiring standard +5, +12 power supplies, the FD179X is available in a standard 40-pin dual-in-line package.

The FD179X Family consists of 6 devices. The differences between these devices is summarized in Figure 1. The 1792 and 1794 are "single density only" devices, with the Double Density Enable pin ($\overline{DDEN}$) left open by the user. Both True and inverted Data Bus devices are available. Since the 179X can only drive one TTL Load, a true data bus system may use the 1791 with external inverting buffers to arrive at a true bus scheme. The 1795 and 1797 are identical to the 1791 and 1793, except a side select output has been added that is controlled through the Command Register.

## SYSTEM DESIGN

The first consideration in Floppy Disk Design is to determine which type of drive to use. The choice ranges from single-density single sided mini-floppy to the 8" double-density double-sided drive. Figure 2 illustrates the various drive and data capacities associated with each type. Although the 8" double-density drive offers twice as much storage, a more complex data separator and the addition of Write Precompensation circuits are mandatory for reliable data transfers. Whether to go with 8" double-density or not is dependent upon PC board space and the additional circuitry needed to accurately recover data with extreme bit shifts. The byte transfer time defines the nominal time required to transfer one byte of data from the drive. If the CPU used cannot service a byte in this time, then a DMA scheme will probably be required. The 179X also needs a few microseconds for overhead, which is subtracted from the transfer time. Figure 3 shows the actual service times that the CPU must provide on a byte-by-byte basis. If these times are not met, bytes of data will be lost during a read or write operation. For each byte transferred, the 179X generates a DRQ (Data Request) signal on Pin 38. A bit is provided in the Status Register which is also set upon receipt of a byte from the Disk. The user has the option of reading the status register through program control or using the DRQ Line with DMA or interrupt schemes. When the data register is read, both the Status Register DRQ bit and the DRQ Line are automatically reset. The next full byte will again set the DRQ and the process continues until the sector(s) are read. The Write operation works exactly the same way, except a WRITE to the Data Register causes a reset of both DRQ's.

## RECORDING FORMATS

The FD179X accepts data from the disk in a Frequency- Modulated (FM) or Modified-Frequency-Modulated (MFM) Format. Shown in Figures 4A and 4B are both these Formats when writing a hexidecimal byte of 'D2.' In the FM mode, the 8 bits of data are broken up into "bit cells." Each bit cell begins with a clock pulse and the center of the bit cell defines the data. If the data bit = 0, no pulse is written; if the data = 1, a pulse is written in the center of the cell. For the 8" drive, each clock is written 4 microseconds apart.



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In the MFM mode, clocks are decoded into the data stream. The byte is again broken up into bit cells, with the data bit written in the center of the bit cell if data = 1. Clocks are only written if both surrounding data bits are zero. Figure 4B shows that this occurs only once between bit cell 4 and 5. Using this encoding scheme, pulses can occur 2, 3 or 4 microseconds apart. The bit cell time is now 2 microseconds; twice as much data can be recorded without increasing the Frequency rate due to the encoding scheme.

The 179X was designed to be compatible with the IBM 3740 (FM) and System 34 (MFM) Formats. Although most users do not have a need for data exchange with IBM mainframes, taking advantage of these well studied formats will ensure a high degree of system performance. The 179X will allow a change in gap fields and sector lengths to increase usable storage capacity, but variations away from these standards is not recommended. Both IBM standards are soft-sector format. Because of the wide variation in address marks, the 179X can only support soft-sectored media. Hard sectored diskettes have continued to lose popularity, mainly due to the unavailability of a standard and the limitation of sector lengths imposed by the physical sector holes in the diskette.

**PROCESSOR INTERFACE**

The Interface of the 179X to the CPU consists of an 8-bit Bi-directional bus, read/write controls and optional interrupt lines. By selecting the device via the CHIP SELECT Line, each of the five internal registers can be accessed.

Shown below are the registers and their addresses:

| PIN 3 CS | PIN 6 $A_1$ | PIN 5 $A_0$ | PIN 4 $\overline{RE} = 0$ | PIN 2 $\overline{WE} = 0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | STATUS REG | COMMAND |
| 0 | 0 | 1 | TRACK REG | REG |
| 0 | 1 | 0 | SECTOR REG | TRACK REG |
| 0 | 1 | 1 | DATA REG | SECTOR REG |
| 1 | X | X | H1-Z | DATA REG |
| | | | | H1-Z |

Each time a command is issued to the 179X, the Busy Bit is set and the INTRQ (Interrupt Request) Line is reset. The user has the option of checking the Busy Bit or use the INTRQ Line to denote command completion. The Busy Bit will be reset whenever the 179X is idle and awaiting a new command. The INTRQ Line, once set, can only be reset by a READ of the Status Register or issuing a new command. The MR (Master Reset) Line does not affect INTRQ.

The $A_0$, $A_1$, Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU address lines, in which case the 179X will be memory-mapped and addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6820, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the 179X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

| OPERATION | NEXT OPERATION | DELAY REQ'D |
|---|---|---|
| WRITE TO COMMAND REG | READ STATUS REGISTER | MFM = 14$\mu$ s* FM = 28$\mu$ s |
| WRITE TO ANY REGISTER | READ FROM A DIFFERENT REG | NO DELAY |

*NOTE: Times Double when CLK = 1MHz (5¼" drive).

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2 MHz (8" drive) or 1 MHz (5 ¼" drive) with a 50% duty cycle. Accuracy should be +1% (crystal source) since all internal timing, including stepping rates, are based upon this clock.

The $\overline{MR}$ or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a Restore Command (Hex '03') on the rising edge. A quicker stepping rate can be written to the Command Register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The 179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TR00}$ line to go active low. This line should be connected to the drive's $\overline{TR00}$ sensor.

The $\overline{DDEN}$ line causes selection of either single density ($\overline{DDEN}$ = 1) or double density operation. $\overline{DDEN}$ should not be switched during a read or write operation.



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## FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the 179X. Inputs to the 179X may be buffered or tied to the drive's outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed -0.3 volts, while integrity of $V_{IH}$ and $V_{OH}$ levels should be kept within spec.

## MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with a period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{IP}$ or Index Pulse. This Line is tied to the drives Index L.E.D. sensor and makes an active transition for each revolution of the diskette. The $\overline{TR00}$ Line is another L.E.D. sensor that informs the 179X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open," Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The 179X will look at the ready signal prior to executing READ/WRITE commands. READY is *not* inspected during any Type I commands. All Type I commands will execute regardless of the Logic Level on this Line.

## WRITE SIGNALS

Writing of data is accomplished by the use of the WD, WG, WF, TG43, EARLY and LATE Lines. The WG or Write Gate Line is used to enable write current at the drive's R/W head. It is made active prior to writing data on the disk. The WF or WRITE FAULT Line is used to inform the 179X of a failure in drive electronics. This signal is multiplexed with the VFOE Line and must be logically separated if required. Figure 5 illustrates three methods of demultiplexing.

The TG43 or "TRACK GREATER than 43" Line is used to decrease the Write Current on the inner tracks, where bit densities are the highest. If not required on the drive, TG43 may be left open.

## WRITE PRECOMPENSATION

The 179X provides three signals for double density Write Precompensation use. These signals are WRITE DATA, EARLY and LATE. When using single density drives (eighter 8" or 5 1/4"), Write Precompensation is not necessary and the WRITE DATA line is generally TTL Buffered and sent directly to the drive. In this mode, EARLY and LATE are left open.

For double density use, Write Precompensation is a function of the drive. Some manufacturers recommend Precompensating the 5 1/4" drive, while others do not.

With the 8" drive, Precompensation may be specified from TRACK 43 on, or in most cases, all TRACKS. If the recommended Precompensation is not specified, check with the manufacturer for the proper configuration required.

The amount of Precompensation time also varies. A typical value will usually be specified from 100-300ns. Regardless of the parameters used, Write Precompensation must be done external to the 179X. When DDEN is tied low, EARLY or LATE will be activated at least 125ns. before and after the Write Data pulse. An Algorithm internal to the 179X decides whether to raise EARLY or LATE, depending upon the previous bit pattern sent. As an example, suppose the recommended Precomp value has been specified at 150ns. The following action should be taken:

| EARLY | LATE | ACTION TAKEN |
|---|---|---|
| 0 | 0 | delay WD by 150 ns (nominal) |
| 0 | 1 | delay WD by 300ns (2X value) |
| 1 | 0 | do not delay WD |

There are two methods of performing Write Precompensation:

1) External Delay elements
2) Digitally

Shown in Figure 6 is a Precomp circuit using the Western Digital 2143 clock generator as the delay element. The WD pulse from the 179X creates a strobe to the 2143, causing subsequent output pulses on the 01, 02 and 03 signals. The 5K Precomp adjust sets the desired Precomp value. Depending upon the condition of EARLY and LATE, 01 will be used for EARLY, 02 for nominal (EARLY = LATE = 0), and 03 for LATE. The use of "one-shots" or delay line in a Write Precompensation scheme offers the user the ability to vary the Precomp value. The 04 output resets the 74LS175 Latch in anticipation of the next WD pulse. Figure 7 shows the WD-EARLY/LATE relationship, while Figure 8 shows the timing of this write Precomp scheme.

Another method of Precomp is to perform the function digitally. Figure 9 illustrates a relationship between the WD pulse and the CLK pin, allowing a digital Precomp scheme. Figure 10 shows such a scheme with a preset Write Precompensation value of 250ns. The synchronous counter is used to generate 2 MHz and 4 MHz clock signals. The 2MHz clock is sent to the CLK input of the 179X and the 4 MHz is used by the 4-bit shift register. When a WD pulse is not present, the 4 MHz clock is shifting "ones" through the shift register and maintaining $Q_D$ at a zero level. When a WD pulse is present, a zero is loaded at either A, B, or C depending upon the states of LATE, EN PRECOMP and EARLY. The zero is then shifted by the 4 MHz clock until it reaches the $Q_D$ output. The number of shift operations determines whether the WRITE DATA pulse is written early, nominal or late. If both FM and MFM operations is a system requirement, the output of this circuit should be disabled and the WD pulse should be sent directly to the drive.



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**DATA SEPARATION**

The 179X has two inputs (RAW READ & RCLK) and one output (VFOE) for use by an external data separator. The RAW READ input must present clock and data pulses to the 179X, while the RCLK input provides a "window" or strobe signal to clock each RAW READ pulse into the device. An ideal Data Separator would have the leading edge of the RAW READ pulse occur in the exact center of the RCLK strobe.

Motor Speed Variation. Bit shifts and read amplifier recovery circuits all cause the RAW READ pulses to drift away from their nominal positions. As this occurs, the RAW READ pulses will shift left or right with respect to RCLK. Eventually, a pulse will make its transition outside of its RCLK window, causing either a CRC error or a Record-Not-Found error at the 179X.

A Phase-Lock-Loop circuit is one method of achieving synchronization between the RCLK and RAW READ signals. As RAW READ pulses are fed to the PLL, minor adjustments of the free-running RCLK frequency can be made. If pulses are occurring too far apart, the RCLK frequency is *decreased* to keep synchronization. If pulses begin to occur closer together, RCLK is *increased* until this new higher frequency is achieved. In normal read operations, RCLK will be constantly adjusted in an attempt to match the incoming RAW READ frequency.

Another method of Data Separation is the Counter-Separator technique. The RCLK signal is again free-running at a nominal rate, until a RAW READ pulse occurs. The Separator then denotes the position of the pulse with respect to RCLK (by the counter value), and counts down to increase or decrease the current RCLK window. The next RCLK window will occur at a nominal rate and will continue to run at this frequency until another RAW READ pulse adjusts RCLK, but only the present window is adjusted.

Both PPL and Counter/Separator are acceptable methods of Data Separation. The PPL has the highest reliability because of its "tracking" capability and is recommended for 8" double density designs.

As a final note, the term "Data Separator" may be misleading, since the physical separation of clock and data bits are not actually performed. This term is used throughout the industry, and can better be described as a "Data Recovery Circuit" rather than a Data Separator.

The VFOE signal is an output from the 179X that signifies the head has been loaded and valid data pulses are appearing on the RAW READ line. It can be used to enable the Data Separator and to insure clean RCLK transitions to the 179X. Since some drives will output random pulses when the head is disengaged, VFOE can prevent an erratic RCLK signal during this time. If the Data Separator requires synchronization during a known pattern of one's or zero's, then RG (READ GATE) can be used. The RG signal will go active when the 179X is currently over a field of zero's or ones. RG is not available on the 1795/1797 devices, since this signal was replaced with the SSO (Side Select Output) Line.

Shown in Figure 11 is a 2½ IC Counter/Separator. The 74LS193 free runs at a frequency determined by the CRYCLK input. When a RAW READ pulse occurs, the counter is loaded with a starting count of 5. When the RAW READ Line returns to a Logic 1, the counter counts down to zero and again free runs. The 74LS74 insures a 50% duty cycle to the 179X and performs a divide-by-two of the $\overline{CT_D}$ output.

Figure 12 illustrates another Counter/Separator utilizing a PROM as the count generator. Depending upon the RAW READ phase relationship to RCLK, the PROM is addressed and its data output is used as the counter value. A 16 MHz clock is required for 8" double density, while an 8 MHz clock can be used for single density.

Figure 13 shows a Phase-Lock-Loop data recovery circuit. The phase detector (U2, Figure 2) compares the phase of the SHAPED DATA pulse to the phase of VFO CLK 2. If VFO CLK 2 is lagging the SHAPED DATA pulse an output pulse on #9, U2 is generated. The filter/amplifier converts this pulse into a DC signal which increases the frequency of the VCO.

If, correspondingly, CLK 2 is leading the SHAPED DATA pulse, an output pulse on #5, U2 is generated. This pulse is converted into a DC signal which decreases the frequency of the VCO. These two actions cause the VCO to track the frequency of the incoming READ DATA pulses. This correction process to keep the two signals in phase is constantly occurring because of spindle speed variation and circuit parameter variations.

The operating specifications for this circuit are as follows:

| | |
|---|---|
| Free Running Frequency | 2 MHz |
| Capture Range | ± 15% |
| Lock Up Time | 50 microsec. "1111" or "0000" Pattern<br>100 Microsec "1010" Pattern |

The RAW READ pulses are generated from the falling edge of the SHAPED DATA pulses. The pulses are also reshaped to meet the 179X requirements. VFO CLK 2 OR 4 is divided by 2 once again to obtain VFO CLK OUT whose frequency is that required by the 179X RCLK input. RCLK must be controlled by VFOE so VFOE is sampled on each rising edge of VFO CLK OUT. When VFOE goes active EN RCLK goes active in synchronization with VFO CLK OUT preventing any glitches on the RCLK output. When VFOE goes inactive EN RCLK goes inactive in synchronization with VFO CLK OUT, again preventing any glitches on the RCLK output.

Figure 14 illustrates a PPL data recovery circuit using the Western Digital 1691 Floppy Support device. Both data recovery and Write Precomp Logic is contained within the 1691, allowing low chip count and PLL



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reliability. The 74S124 supplies the free-running VCO output. The PUMP UP and PUMP DOWN signals from the 1691 are used to control the 74S124's frequency.

**COMMAND USAGE**

Whenever a command is successfully or unsuccessfully completed, the busy bit of the Status Register is reset and the INTRQ line is forced high. Command termination may be detected either way. The INTRQ can be tied to the host processor's interrupt with an appropriate service routine to terminate commands. The busy bit may be monitored with a user program and will achieve the same results through software. Performing both an INTRQ and a busy bit check is not recommended because a read of the Status Register to determine the condition of the busy bit will reset the INTRQ line. This can cause an INTRQ from not occurring.

**RESTORE COMMAND**

On some disk drives, it is possible to position the R/W head outward past Track 00 and prevent the TR00 line from going low unless a STEP IN is first performed. If this condition exists in the drive used, the RESTORE command will never detect a TR00. Issuing several STEP IN pulses before a RESTORE command will remedy this situation. The RESTORE and all other Type I commands will execute even though the READY bit indicates the drive is not ready (NOT READY = 1).

**READ TRACK COMMAND**

The READ TRACK command can be used to manually inspect data on a hard copy printout. Gaps, address marks and all data are brought in to the Data Register during this command. The READ TRACK command may be used to inspect diskettes for valid formatting and data fields as well as address marks. Since the 179X does not synchronize clock and data until the Index Address Mark is detected, data previous to this ID mark will not be valid. READ GATE (RG) is not actuated during this command.

**READ ADDRESS COMMAND**

In systems that use either multiple drives or sides, the read address command can be used to tell the host processor which drive or side is selected. The current position of the R/W head is also denoted in the six bytes of data that are sent to the computer.

| TRACK SIDE | SECTOR | CRS LENGTH | CRC 1 | CRC 2 |
|---|---|---|---|---|

The READ ADDRESS command as well as all other Type II and Type III commands will not execute if the READY line is inactive (READY = 0). Instead, an interrupt will be generated and the NOT READY status bit will be set to a 1.

**FORCED INTERRUPT COMMAND**

The Forced Interrupt command is generally used to terminate a multiple sector command or to insure Type I status in the Status Register. The lower four bits of the command determine the conditional interrupt as follows:

$I_0$ = NOT-READY TO READY TRANSITION
$I_1$ = READY TO NOT-READY TRANSITION
$I_2$ = EVERY INDEX PULSE
$I_3$ = IMMEDIATE INTERRUPT

Regardless of the conditional interrupt set, any command that is currently being executed when the Forced Interrupt command is loaded will immediately be terminated and the Busy Bit will be reset indicating an idle condition.

Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occured.

The conditional interrupt is enabled when the corresponding bit positions of the command (I3 - I0) are set to a 1. If $I_3$ - $I_0$ are all set to zero, no interrupt will occur, but any command presently under execution will be immediately terminated upon receipt of the Force Interrupt command (HEX D0).

As usual, to clear the interrupt a read of the Status Register or a write to the command register is required. The exception is when using the immediate interrupt condition ($I_3$ = 1). If this command is loaded into the command register, an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt; another forced interrupt command with $I_3$ - $I_0$ = 0 must be loaded into the command register in order to reset the INTRQ from this condition.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition $I_1$ = 1 and the Every Index Pulse $I_2$ = 1 are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

**DATA RECOVERY**

Occasionally, the R/W head of the disk drive may get "off track", and dust and dirt may get trapped on the media. Both of these conditions will cause a RECORD NOT FOUND and/or a CRC error to occur. This "soft error" can usually be recovered by the following procedure:

1. Issue the command again
2. Unload and load the head and repeat step
3. Issue a restore, seek the track, and repeat step 1

If RNF or CRC errors are still occurring after trying these methods, a "hard error" may exist. This is usually caused by improper disk handling, exposure to high magnetic fields, etc. and generally results in destroying portions or tracks of the diskette.



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**FIGURE 1. DEVICE CHARACTERISTICS**

| DEVICE | SNGL DENSITY | DBLE DENSITY | INVERTED BUS | TRUE BUS | DOUBLE-SIDED |
|---|---|---|---|---|---|
| 1791 | X | X | X | | |
| 1792 | X | | X | | |
| 1793 | X | X | | X | |
| 1794 | X | | | X | |
| 1795 | X | X | X | | X |
| 1797 | X | X | | X | X |

**FIGURE 2. STORAGE CAPACITIES**

| SIZE | DENSITY | SIDES | UNFORMATTED CAPACITY (NOMINAL) | | BYTE TRANSFER TIME | FORMATTED CAPACITY | |
|---|---|---|---|---|---|---|---|
| | | | PER TRACK | PER DISK | | PER TRACK | PER DISK |
| 5 1/4" | SINGLE | 1 | 3125 | 109,375* | 64μs | 2304** | 80,640 |
| 5 1/4" | DOUBLE | 1 | 6250 | 218,750 | 32μs | 4608*** | 161,280 |
| 5 1/4" | SINGLE | 2 | 3125 | 218,750 | 64μs | 2304 | 161,280 |
| 5 1/4" | DOUBLE | 2 | 6250 | 437,500 | 32μs | 4608 | 322,560 |
| 8" | SINGLE | 1 | 5208 | 401,016 | 32μs | 3328 | 256,256 |
| 8" | DOUBLE | 1 | 10,416 | 802,032 | 16μs | 6656 | 512,512 |
| 8" | SINGLE | 2 | 5208 | 802,032 | 32μs | 3328 | 512,512 |
| 8" | DOUBLE | 2 | 10,416 | 1,604,064 | 16μs | 6656 | 1,025,024 |

*Based on 35 Tracks/Side.
**Based on 18 Sectors/Track (128 byte/sec).
***Based on 18 Sectors/Track (256 bytes/sec).



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**FIGURE 3. NOMINAL VS. WORST CASE SERVICE TIME**

| SIZE | DENSITY | NOMINAL TRANSFER TIME | WORST-CASE 179X SERVICE TIME | |
|---|---|---|---|---|
| | | | READ | WRITE |
| 5 1/4" | SINGLE | 64μs | 55.0μs | 47.0μs |
| 5 1/4" | DOUBLE | 32μs | 27.5μs | 23.5μs |
| 8" | SINGLE | 32μs | 27.5μs | 23.5μs |
| 8" | DOUBLE | 16μs | 13.5μs | 11.5μs |

**FIGURE 4A. FM RECORDING**

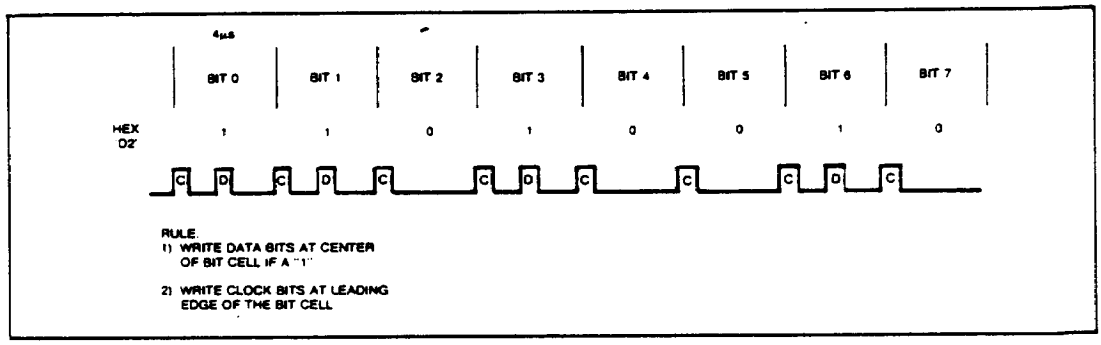


**FIGURE 4B. MFM RECORDING**

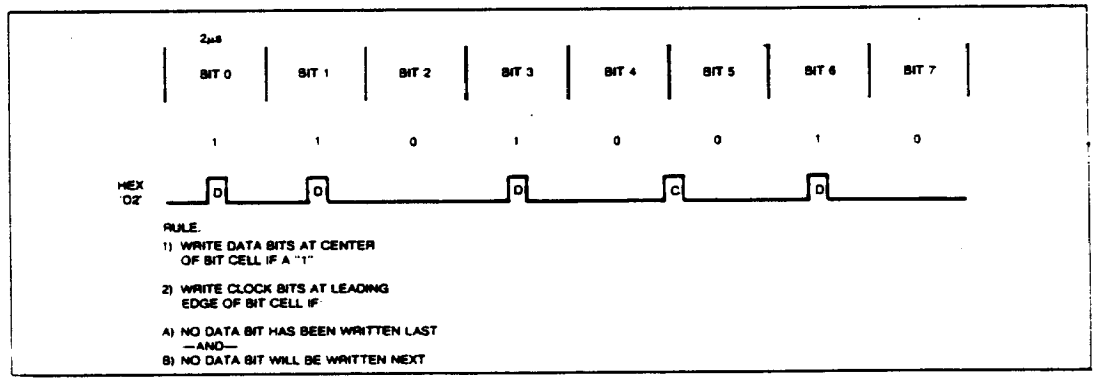




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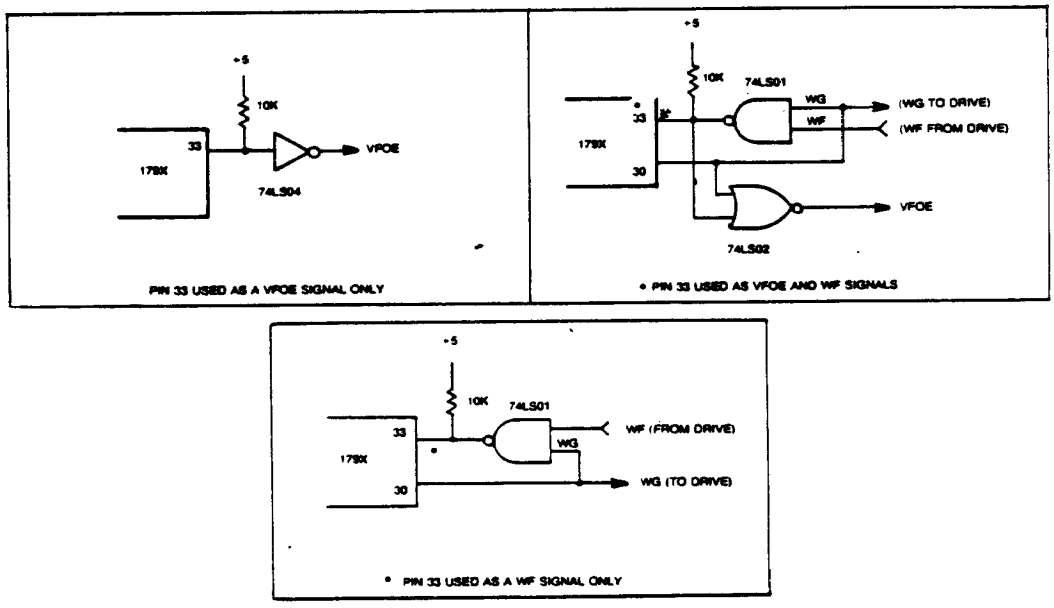
**FIGURE 5. WF / VFOE DEMULTIPLEXING CIRCUITRY**



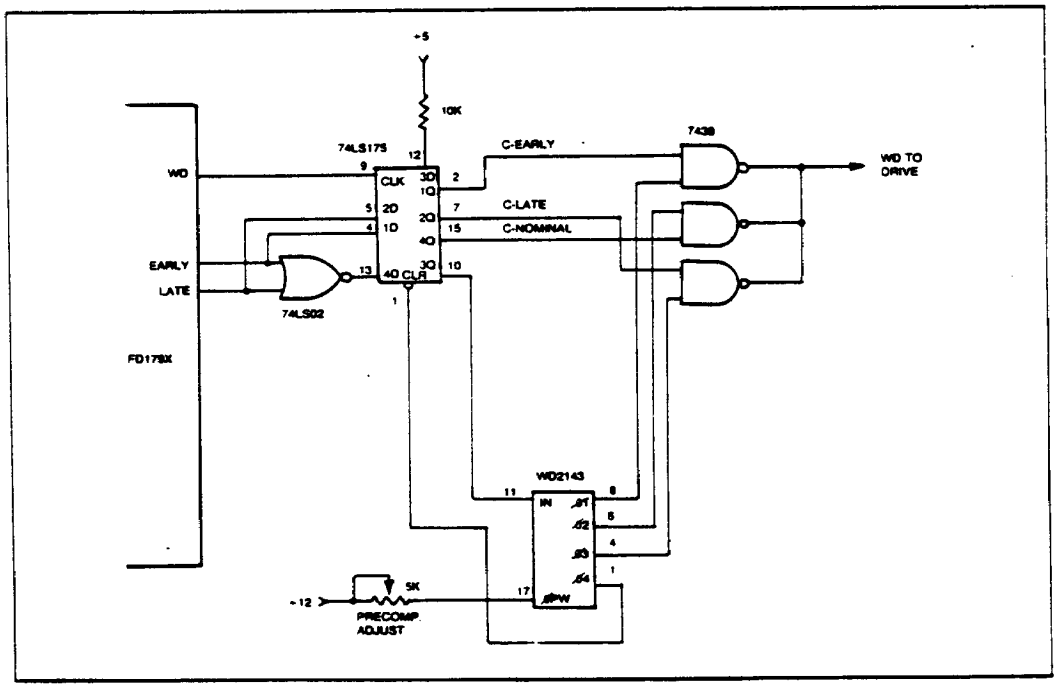




**FIGURE 6. 179X WRITE PRE-COMP**



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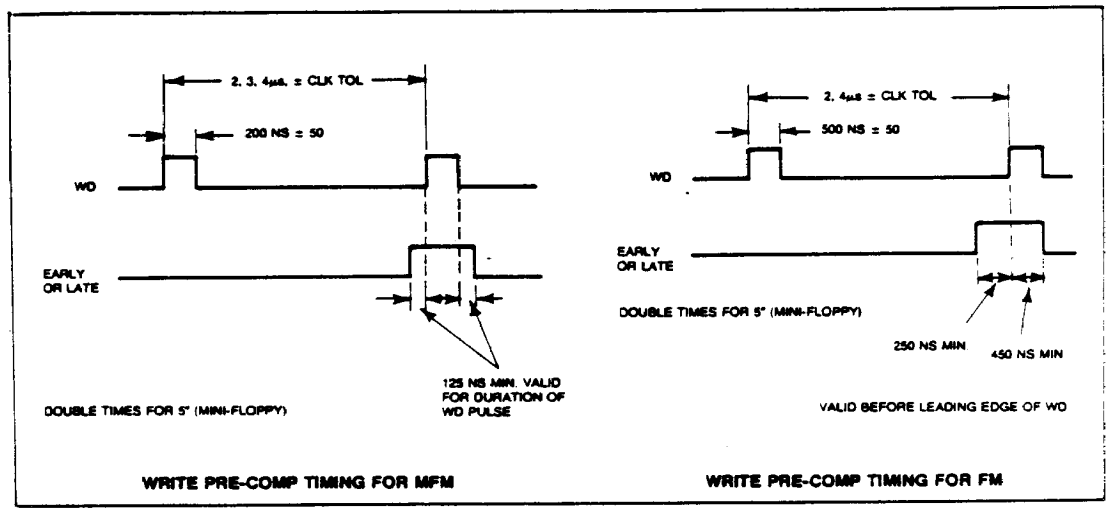


FIGURE 7. WRITE PRE-COMP TIMING

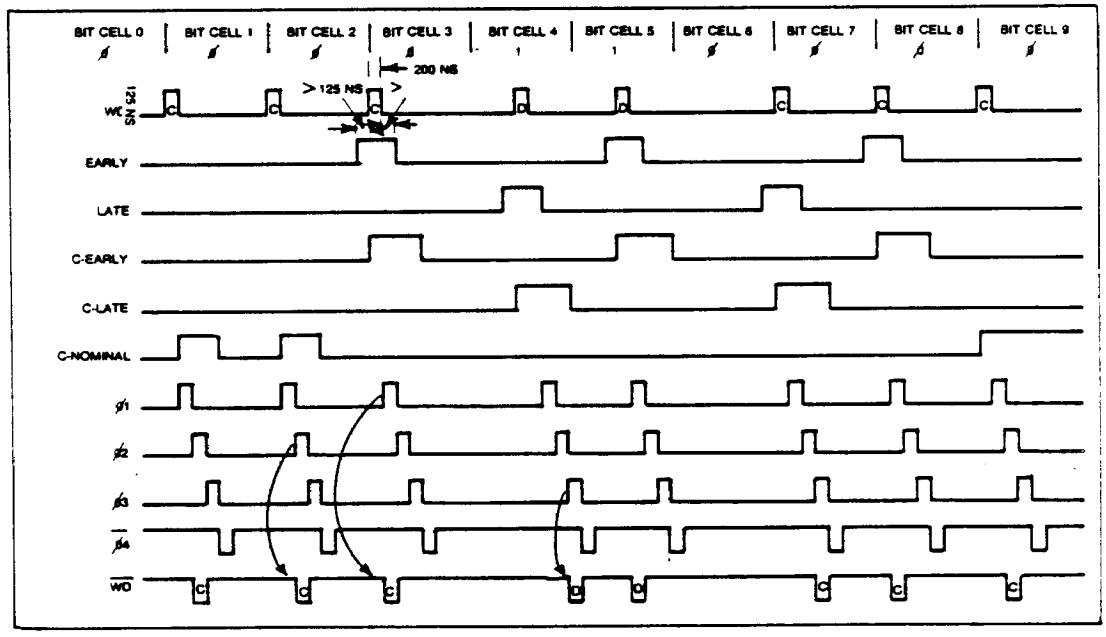


FIGURE 8. PRE-COMP TIMING FOR CIRCUIT IN FIGURE 6



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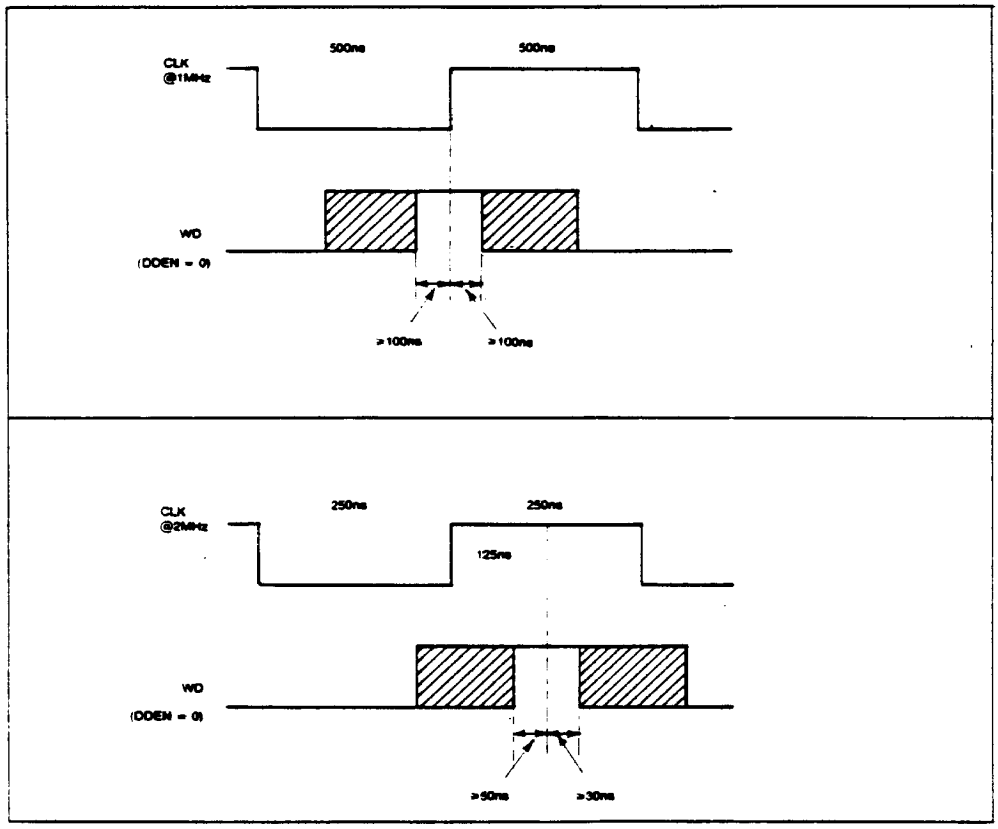


FIGURE 9. WD/CLK RELATIONSHIP FOR WRITE PRECOMP USE

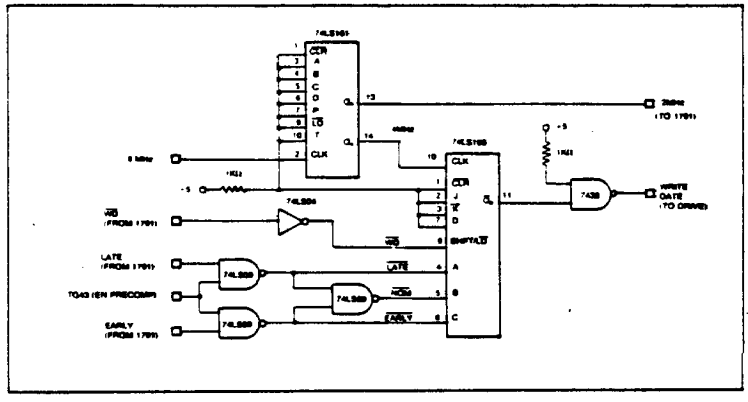

FIGURE 10. DIGITAL WRITE PRECOMP CIRCUIT
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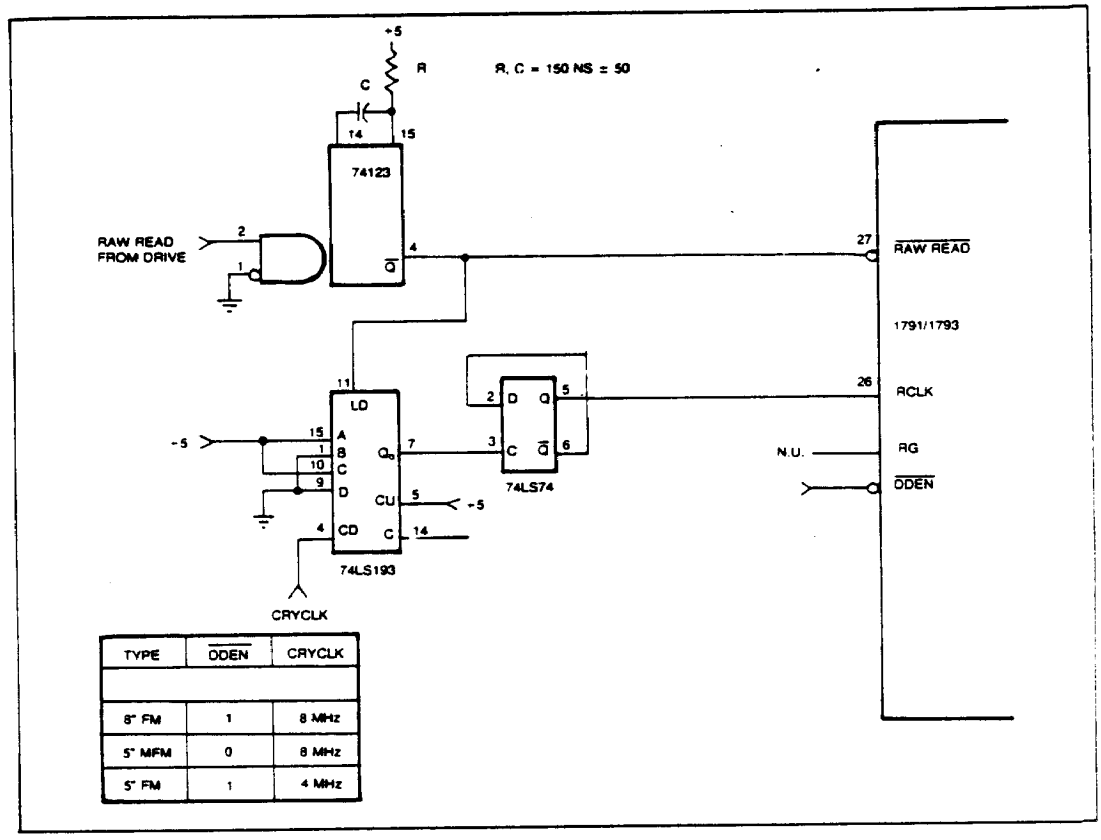


| TYPE | $\overline{\text{ODEN}}$ | CRYCLK |
|---|---|---|
| | | |
| 8" FM | 1 | 8 MHz |
| 5" MFM | 0 | 8 MHz |
| 5" FM | 1 | 4 MHz |

**FIGURE 11. COUNTER / SEPARATOR**



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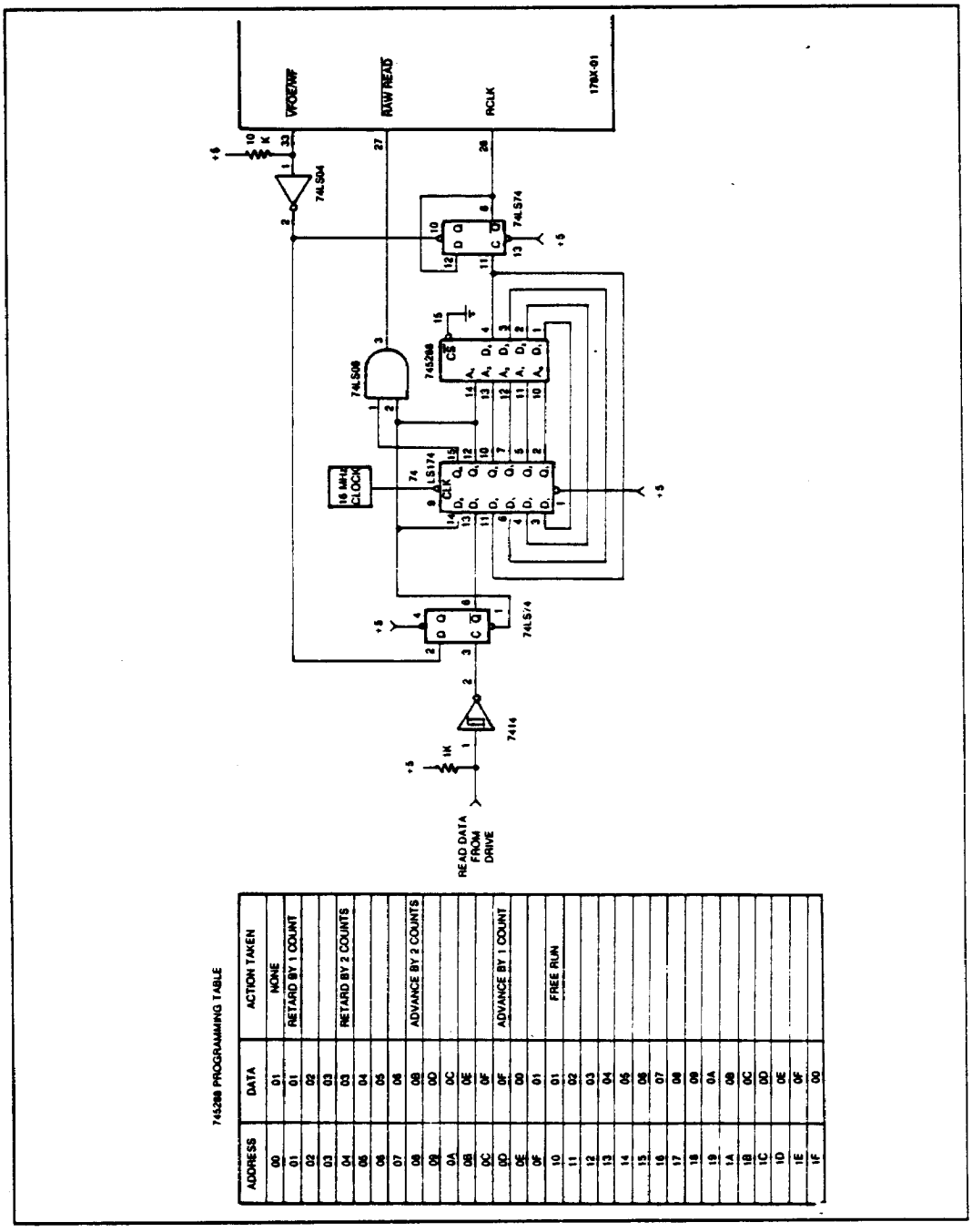


**FIGURE 12. 179X DATA SEPARATOR**
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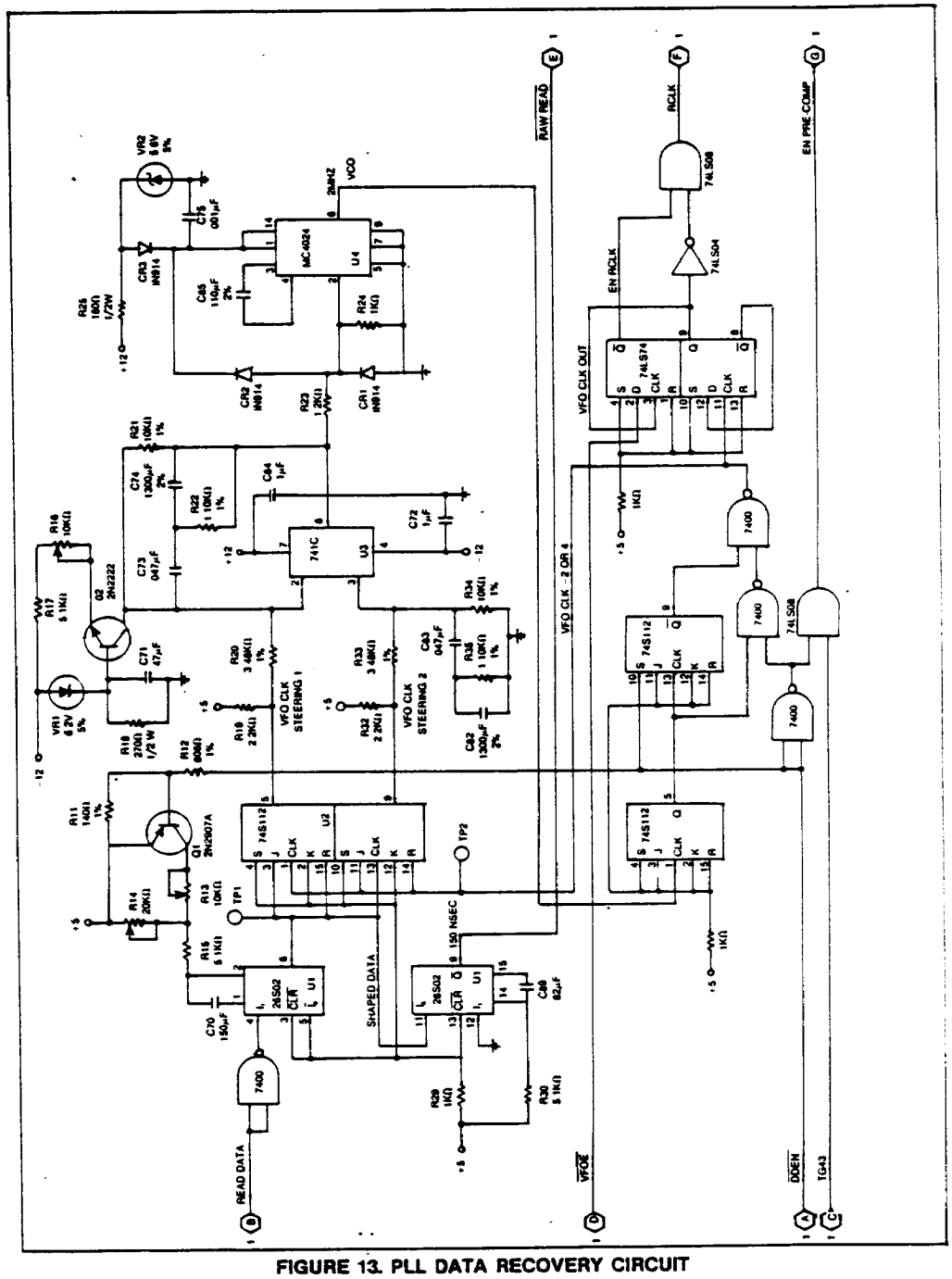


**FIGURE 13. PLL DATA RECOVERY CIRCUIT**
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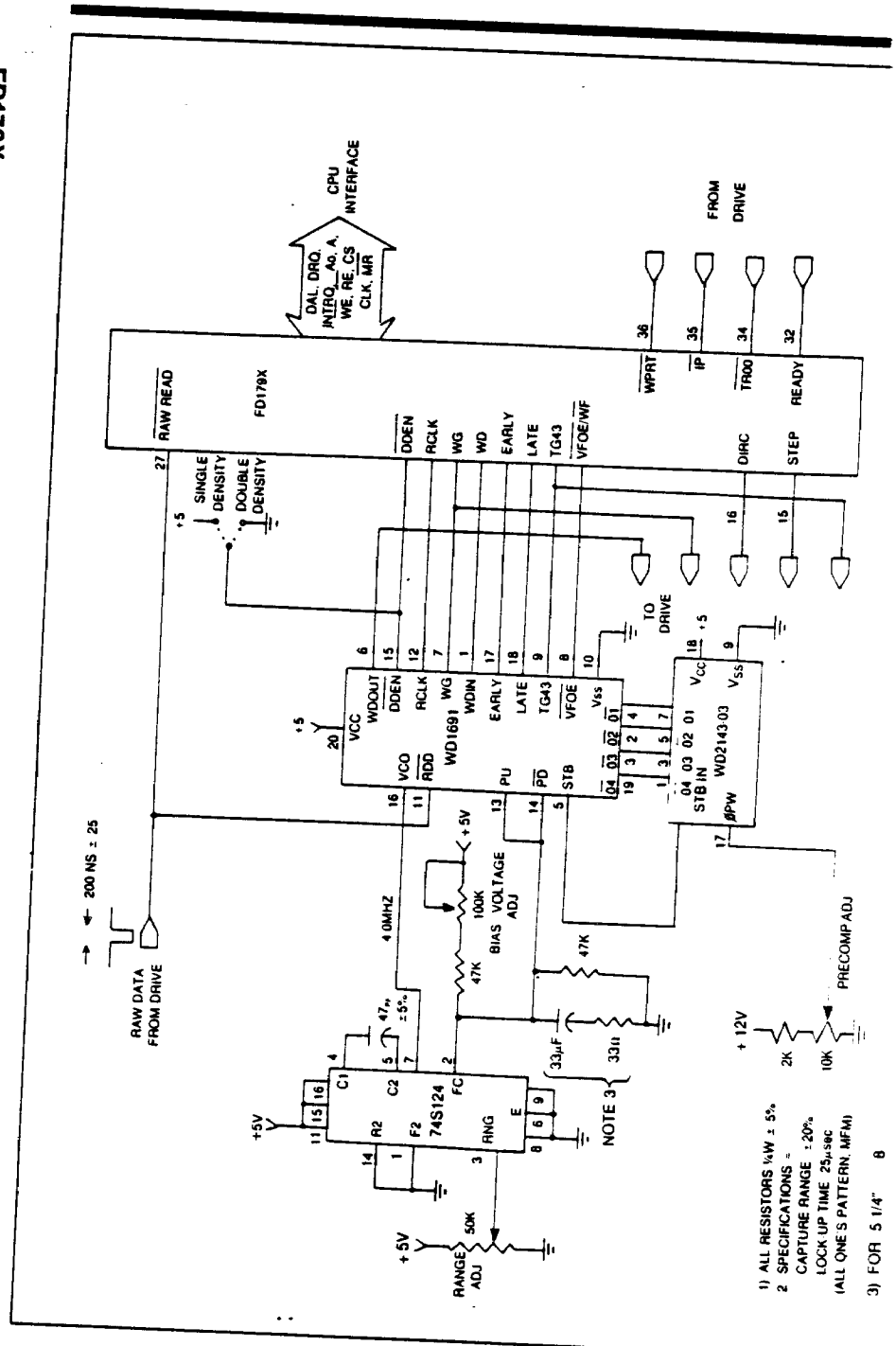


**FIGURE 14. 8" SINGLE / DOUBLE DENSITY SYSTEM**



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