Main differences between I/O Board v3.0 and 1990 version:

· The biggest, most obvious difference is that the 2 SIMM sockets and their supporting logic have been moved off the v3.0 I/O board, and onto the v2.0 Minibus board.

· The rear panel connectors for serial port /t2 (P2), Sound I/O (P6), and Joystick (P8) have been replaced with header connectors.

· 68681 serial port headers for /t3 (P9) and /t4 (P12) have been changed from 8-pin to 10-pin

· The WD33C93 socket has been changed from a 40-pin DIP to a 44-pin PLCC. I was told that the v.3.0 I/O board could support the B model of the WD33C93, which could be faster, though I'm not sure if this has anything to do with the PLCC package.

· The general layout of the board has changed somewhat.

v3.0   1990

P2   /t2, 10pin header, 1488/1489   P2 /t2, DE9M on board, Max233
P9   /t3, 10pin header, 1488/1489   P9 /t3, 8pin header, requires level translator on 'paddle
                                                         board'
P12 /t4, 10pin header, 1488/1489   P12 /t4, 8pin header, requires level translator on 'paddle
                                                         board'

The ADC/DAC chips need -5v. On both versions of the board, this is achieved with a 79L05 voltage regulator. This has to be fed with a negative voltage, at least -8v. This can only come from the -12v supply. So 12v is used on the 1990 I/O board, even if the +12v rail is not used for RS232.

MM-1_3.JPG schematic file does include pins 63 and 64 of P4, bringing +12v to pin 7 (RTS) of /t2 and -12v to pin 2 of the 79L05, which is then regulated to -5v on pin 3.

It looks as if the DRAM refresh / selection circuit is carried over largely intact, even keeping most of the same chip identification designations. If a schematic of the circuit on the 1990 I/O board can be found, that would likely give us a big head start in reversing the circuit as it is on the 8M Minibus 2.0 board.

8M Parts list:

C1-C7:	.1µf ceramic
C8-C10:	10µf tantalum
R1-R4:	4.7k SIP 10 pin resistor network
RN1-RN3:	22Ω SIP 8 pin resistor network
U1:	22V10 25ns PAL/GAL
U2:	74hc4040n
U3:	SIMM
U4:	SIMM
U5:	74act257n
U6:	74act257n
U7:	74act257n
U8:	74hc32n

1990 I/O:

U1:	22V10 25ns PAL/GAL	
U2:	74hc4040n	12bit binary counter
U5:	74ac257n	quad 2ch tristate mux
U6:	74ac257n	quad 2ch tristate mux
U7:	74ac257n	quad 2ch tristate mux
U25:	74hct32	quad 2input OR