Radio Shack®

Service Manual

26-3134/3136

TRS-80®
COLOR COMPUTER 2
NTSC VERSION
Catalog Number: 26-3134/3136

CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

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SECTION I

GENERAL

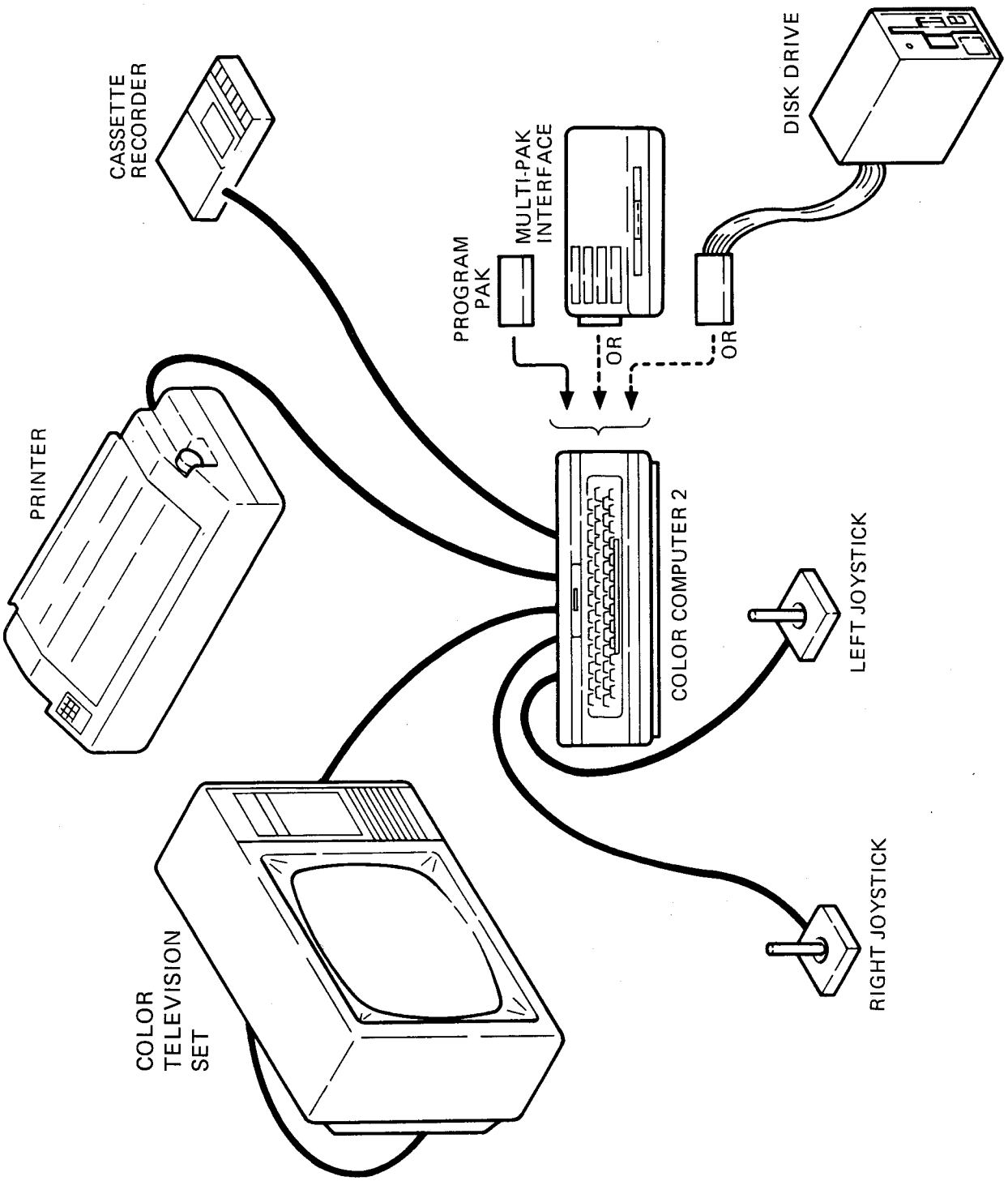


Figure 1-1. Color Computer 2 Installation

1.1 Introduction

The Color Computer 2 is a refined version of Radio Shack's popular Color Computer. It is designed to provide the same reliable operation as its predecessor, but incorporates the latest in electronic technology. Interconnection to a printout device, or modem provides maximum versatility of the Color Computer 2. Figure 1-1 shows a typical installation of the Color Computer 2. Interconnecting cables are noted which provides signal and control transfer between the major components. Always remember to remove all power from the Color Computer 2 prior to installing any peripheral device to prevent damage to the device or the Color Computer 2.

The Color Computer 2 contains an internal BASIC program in ROM which is accessed when the unit is powered up. Other program modules/cartridges may be inserted into the receptacle at the right side of the unit. An optional Multipak Interface module allows up to four program paks to be installed at the same time with selection of the specific module active at any one time selected either by software or by a switch on the Multipak Interface module. Additional peripheral devices, such as an external disk drive, may be added to the Color Computer 2 for additional memory storage and retrieval.

All inputs to or outputs from the Color Computer 2, with the exception of the program module/cartridges, are contained on the rear panel of the unit. These include the joystick inputs (right and left), Serial I/O, Cass I/O, TV output connector, Power ON/OFF switch, and RESET switch. A recessed channel switch (for selecting either channel 3 or 4 on the TV) is also located on the rear panel of the unit.

1.2 System Description

The primary functions of the Color Computer 2 are performed by five 40-pin Large Scale Integration (LSI) chips plus Random Access Memory (RAM) and Read Only Memory (ROM). These five chips are labeled on the Block Diagram as CPU, SAM, VDG, and two PIAs. With only these five chips plus Random Access Memory (RAM), Read Only Memory (ROM), and a power supply, the Color Computer 2 will operate and provide a composite video output. However, to allow communication with the outside world, I/O interfaces must be added.

The main component of any computer system is the Central Processor Unit (CPU, IC9). It is the function of the CPU to provide or request data and select the proper address for this data. In addition, the CPU is capable of performing a limited set of mathematical and logical operations on the data.

ROM (IC12 + IC13 in Extended Basic) has the function of providing the CPU with a predefined set of instructions. Without ROM, the CPU would run wild and randomly execute instructions. In normal operation, the CPU jumps to the start address in ROM after the reset switch has been pressed and then performs the reset program to set up all of the programmable devices. Following this, the BASIC interpreter residing in ROM is in control of the CPU.

RAM (IC14 thru IC21) provides storage for the programs and/or data currently being executed. In the standard unit, these eight ICs are 16K x 1 but may be upgraded to 64K x 1 ICs as an option. (See Paragraph 3.3 for instructions.)
In addition, this same RAM is used to generate the video display. Normally, no conflict will be observed because the program will use one portion of RAM and the display will use another. During normal usage, the BASIC interpreter located in ROM will control the execution of programs located in RAM.

A central component in the Color Computer 2 is the Synchronous Address Multiplexer (SAM, IC22). This chip provides refresh and address multiplexing for the RAM. It also provides all of the system timing and device selection.

The video display generator (VDG, IC8) provides virtually the entire video interface on one chip and allows several alphanumeric and graphic modes. The mode of operation of the VDG is controlled by one of two Peripheral Interface Adapters (PIAs, IC2 and IC7) used in the Color Computer 2. With this information and RAM data, the VDG generates composite video and color information for the modulator circuitry.

The remaining circuitry in the Color Computer 2 is devoted to Input/Output (I/O) communication. The most important part of this circuitry is the keyboard which allows the operator to enter information. Other I/O circuits are provided to allow joystick inputs, cassette input and output, and RS-232C input and output.

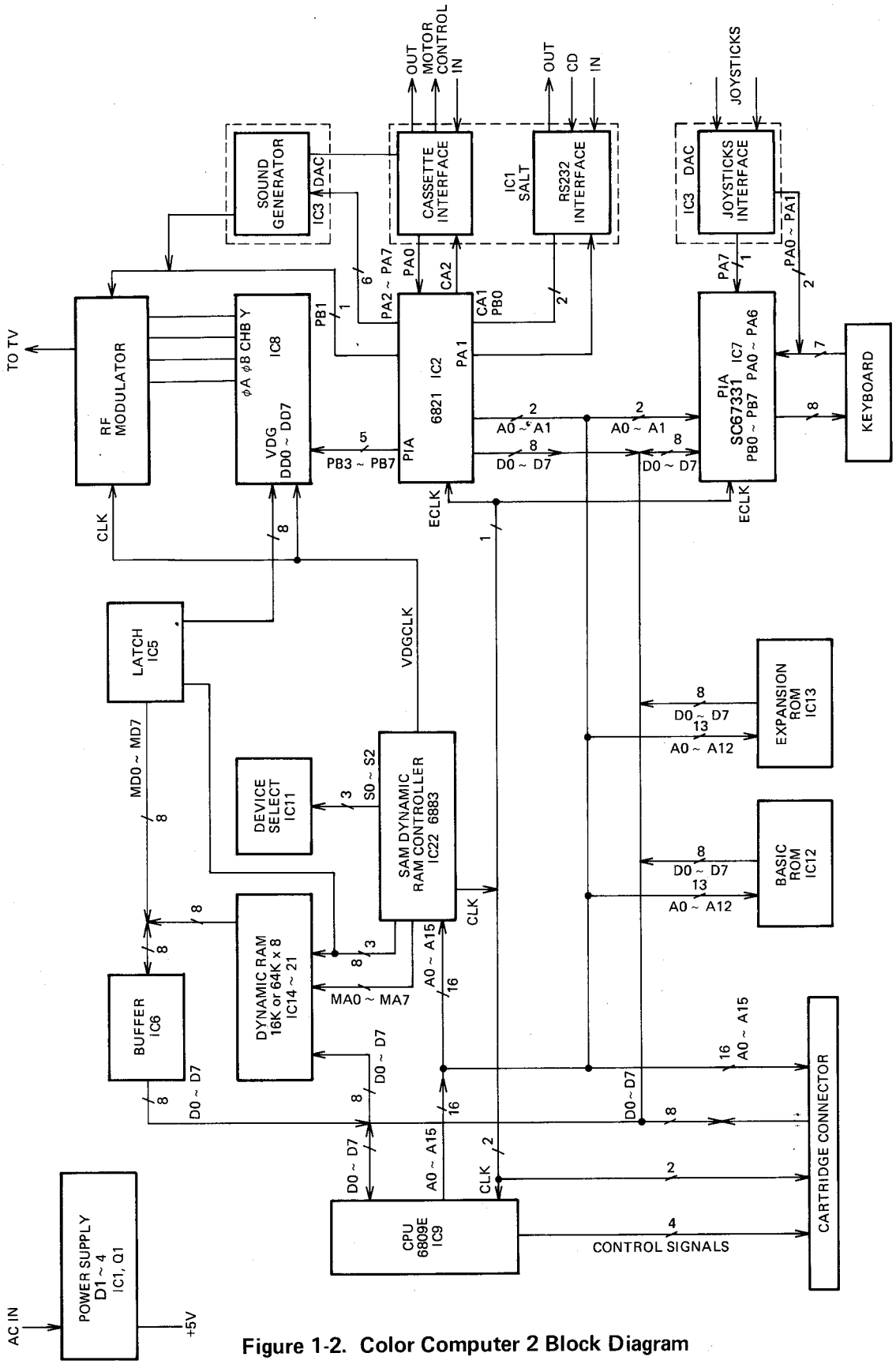


Figure 1-2. Color Computer 2 Block Diagram

1.3 Memory Map

The first page of the Memory Map (Figure 1-3) shows the breakdown of the large blocks of memory in the Color Computer 2. One variable in this block is the video display which may be located anywhere in the memory. BASIC normally locates the video display at the hexadecimal addresses from 0400 to 05FF--cassette only.

The next two pages of the Memory Map explain the addressing for the PIAs. In general, the even numbered memory locations are the I/O registers and the odd numbered memory locations are the control registers. Bit two of the control registers determines what is addressed at the even numbered memory locations. If this bit is set high (logic 1), the data I/O register is addressed. If it is set low, the data direction register is addressed. Normally, the data direction register is addressed only during initialization to allow configuration of the data inputs and outputs. By clearing bit 2 and writing to the even numbered memory location one address below, each bit of the PIA may be set as an input or an output. A 1 in the data direction register sets the bit as an output and a 0 sets the bit as an input.

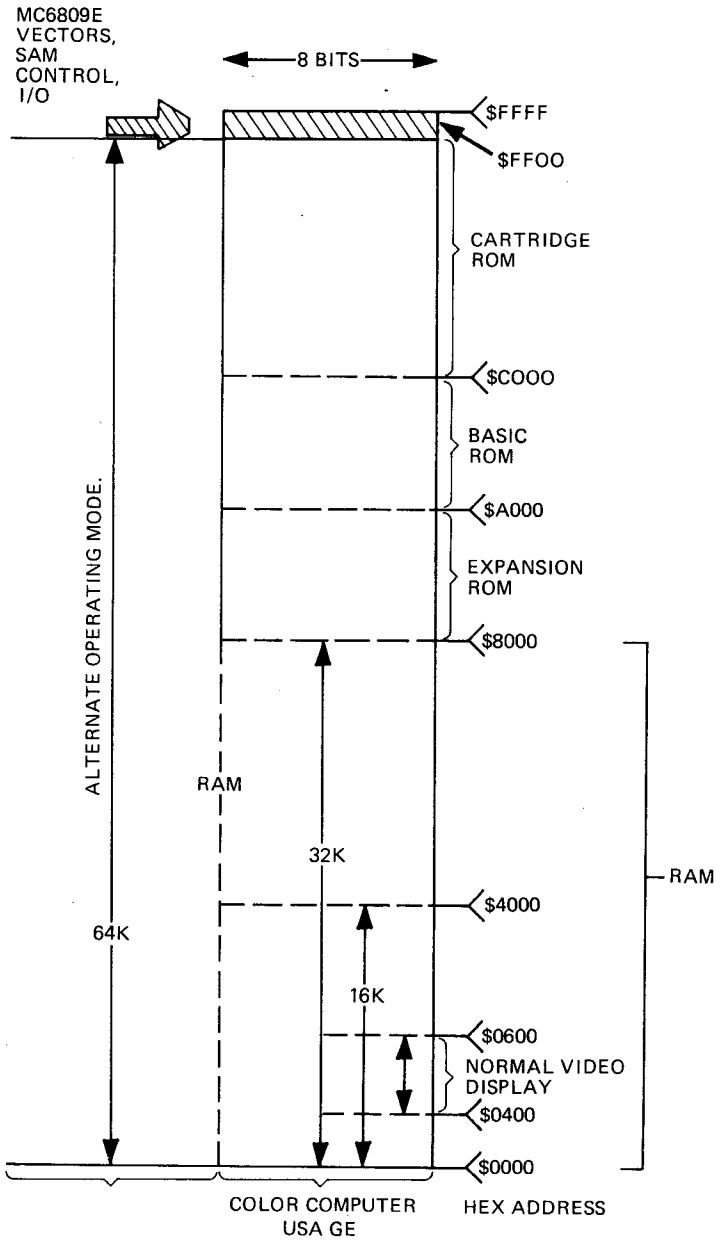


Figure 1-3. Color Computer 2 Memory Map (PAGE 1)

FF00-FF03 PIA IC15

FF00
- BIT 0 = KEYBOARD ROW 1 and right joystick switch
- BIT 1 = KEYBOARD ROW 2 and left joystick switch
- BIT 2 = KEYBOARD ROW 3
- BIT 3 = KEYBOARD ROW 4
- BIT 4 = KEYBOARD ROW 5
- BIT 5 = KEYBOARD ROW 6
- BIT 6 = KEYBOARD ROW 7
- BIT 7 = JOYSTICK COMPARISON INPUT

FF01
- BIT 0 = Control of the Horizontal sync clock (63.5 microseconds) Interrupt Input: 0 = IRQ* to CPU Disabled; 1 = IRQ* to CPU Enabled
- BIT 1 = Interrupt Input: 0 = Flag set on the falling edge of HS; 1 = Flag set on the rising edge of HS
- BIT 2 = Normally 1: 0 = Changes FF00 to the data direction register
- BIT 3 = SEL 1: LSB of the two analog MUX select lines
- BIT 4 = 1 Always
- BIT 5 = 1 Always
- BIT 6 = Not Used
- BIT 7 = Horizontal sync interrupt flag

FF02
- BIT 0 = KEYBOARD COLUMN 1
- BIT 1 = KEYBOARD COLUMN 2
- BIT 2 = KEYBOARD COLUMN 3
- BIT 3 = KEYBOARD COLUMN 4
- BIT 4 = KEYBOARD COLUMN 5
- BIT 5 = KEYBOARD COLUMN 6
- BIT 6 = KEYBOARD COLUMN 7/RAM SIZE OUTPUT
- BIT 7 = KEYBOARD COLUMN 8

FF03
- BIT 0 = Control of the field sync clock 16.667 Ms Interrupt Input: 0 = IRQ* to CPU Disabled; 1 = IRQ* to CPU Enabled
- BIT 1: 0 = sets flag on falling edge FS; 1 = sets flag on rising edge FS
- BIT 2 = NORMALLY 1: 0 = changes FF02 to the data direction register
- BIT 3 = SEL 2: MSB of the two analog MUX select lines
- BIT 4 = 1 Always
- BIT 5 = 1 Always
- BIT 6 = Not Used
- BIT 7 = Field sync interrupt flag

Figure 1-3. Color Computer 2 Memory Map (Cont'd) (PAGE 2)

FF20-FF23 PIA IC14

FF20
- BIT 0 = CASSETTE DATA INPUT
- BIT 1 = RS-232- DATA OUTPUT
- BIT 2 = 6 BIT D/A LSB
- BIT 3 = 6 BIT D/A
- BIT 4 = 6 BIT D/A
- BIT 5 = 6 BIT D/A
- BIT 6 = 6 BIT D/A
- BIT 7 = 6 BIT D/A MSB

FF21
FF21
- BIT 0 — Control of the CD: 0 = FIRQ* to CPU Disabled; 1 = FIRQ* to CPU Enabled
- BIT 1 — RS-232C status Input: 0 = set flag on falling edge CD; 1 = set flag on rising edge CD
- BIT 2 = Normally 1: 0 = changes FF20 to the data direction register
- BIT 3 = Cassette Motor Control: 0 = OFF 1 = ON
- BIT 4 = 1 Always
- BIT 5 = 1 Always
- BIT 6 = Not Used
- BIT 7 = CD Interrupt Flag

FF22
- BIT 0 = RS-232C DATA INPUT
- BIT 1 = SINGLE BIT SOUND OUTPUT
- BIT 2 = RAM SIZE INPUT — HIGH = 16K CHANGEABLE = 64K
- BIT 3 = VDG CONTROL OUTPUT — CSS
- BIT 4 = VDG CONTROL OUTPUT — GM0 & $\overline{INT}$/EXT
- BIT 5 = VDG CONTROL OUTPUT — GM1
- BIT 6 = VDG CONTROL OUTPUT — GM2
- BIT 7 = VDG CONTROL OUTPUT — $\overline{A}$/G

FF23
- BIT 0 — Control of the Cartridge Interrput Input: 0 = FIRQ* to CPU Disabled; 1 = FIRQ* to CPU Enabled
- BIT 1 — 0 = sets flag on falling edge CART*; 1 = sets flag on rising edge CART*
- BIT 2 = Normally 1: 0 = changes FF22 to the data direction register
- BIT 3 = Six BIT Sound Enable
- BIT 4 = 1 Always
- BIT 5 = 1 Always
- BIT 6 = Not Used
- BIT 7 = Cartridge Interrupt Flag

FF40 – FFBF: Not used

Figure 1-3. Color Computer 2 Memory Map (Cont'd) (PAGE 3)

The addresses from FFC0 to FFDF are the control registers for the SAM address multiplexer chip (IC22). There are no data lines to the SAM chip; therefore, two addresses are used to control each register. In general, writing any data to an even numbered memory location will clear the register and writing any data to an odd numbered memory location will set the register. Addresses FFC0-FFC5 control the display mode. To select a certain display mode, the display mode control registers (V0-V2) and the PIA (IC2) controlling the VDG chip must all be set to the proper mode.

Addresses FFC6 to FFD3 control the display starting address. If all of the registers are cleared, the display will begin at 0000. Normally, register F2 will be set causing the display to start at 0400. This feature of the SAM chip allows the display to be paged through all of the RAM. Register P1 controls a feature which is not used in the Color Computer 2. Therefore, it should be cleared at all times.

Addresses FFD6 to FFD9 control the clock speed of the CPU. The Color Computer 2 is designed to operate at 0.89 MHz. Therefore, registers R0 and R1 should be cleared.

Addresses FFDA to FFDD control the memory size setup of the SAM chip. These addresses select 16K or 64K of RAM in the Color Computer 2. This memory size option should be changed only by the reset routine in BASIC. Changes at other times may erase the contents of RAM. Register TY, at addresses FFDE to FFDF, controls the map type. If this bit is cleared, the ROMs occupy the upper 32K of the Memory Map with the lower 32K of address space available for RAM. If this bit is set, the ROMs "disappear" from (are switched out of) the map and all 64K (less the top 256) locations are available for RAM. Caution must be exercised in setting this bit. The control program must be in low memory and must not return to ROM for obvious reasons.

The final series of addresses in the Color Computer 2 are the interrupt and reset vectors. Whenever the CPU receives a reset or interrupt, it will load the address at the indicated location and begin execution at the new location. This dual set of addresses is listed because the vectors are mapped into the top of the BASIC ROM (BFF2-BFFF). For instance, if the CPU reads FFFF it will actually read the contents of BFFF.

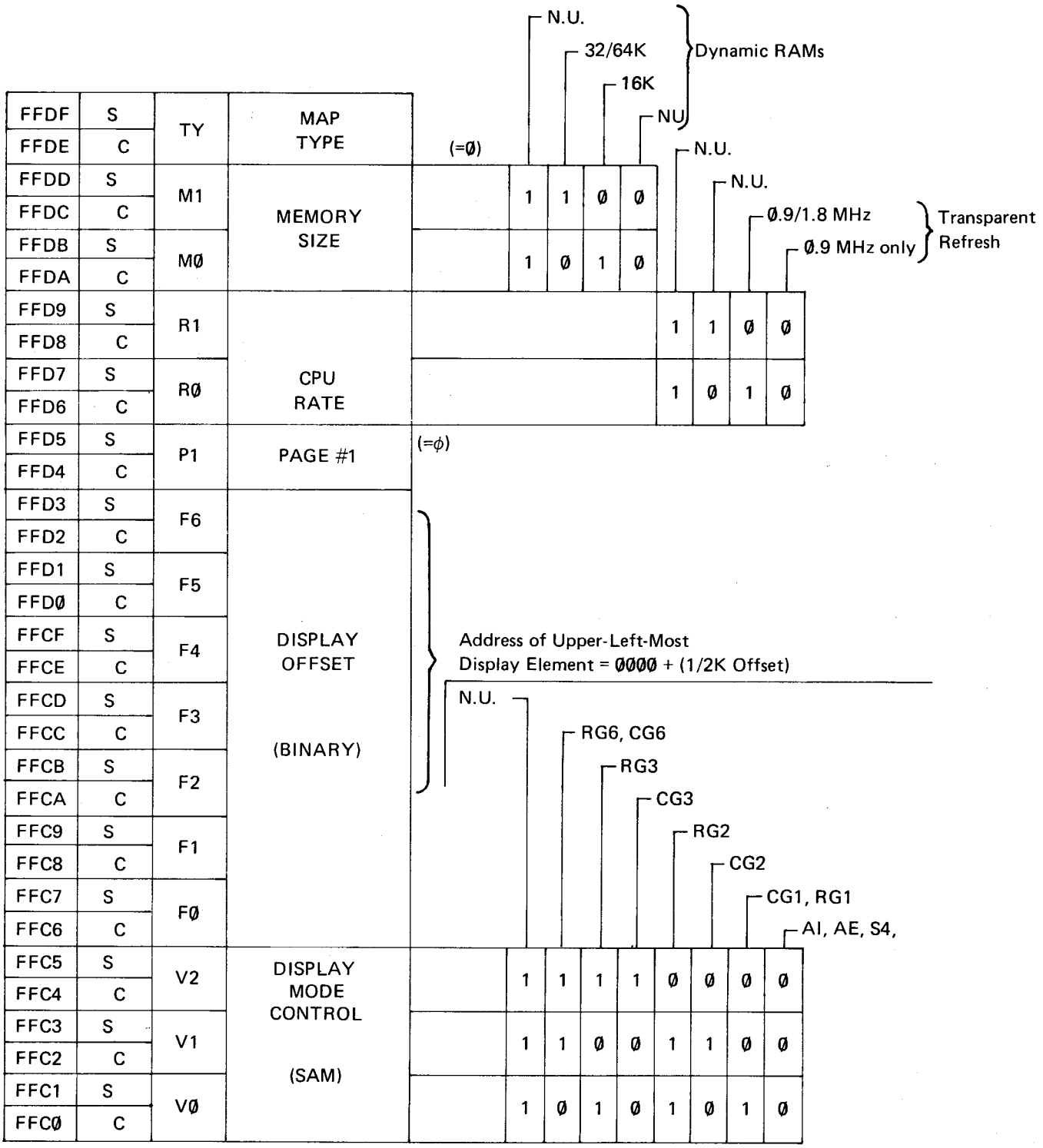


Figure 1-3. Color Computer 2 Memory Map (Cont'd) (PAGE 4)

FFFF OR BFFF		RESET VECTOR LSB
FFFE OR BFFE		RESET VECTOR MSB
FFFD OR BFFD		NMI VECTOR LSB
FFFC OR BFFC		NMI VECTOR MSB
FFFB OR BFFB		SWI1 VECTOR LSB
FFFA OR BFFA		SWI1 VECTOR MSB
FFF9 OR BFF9		IRQ VECTOR LSB
FFF8 OR BFF8		IRQ VECTOR MSB
FFF7 OR BFF7		FIRQ VECTOR LSB
FFF6 OR BFF6		FIRQ VECTOR MSB
FFF5 OR BFF5		SWI2 VECTOR LSB
FFF4 OR BFF4		SWI2 VECTOR MSB
FFF3 OR BFF3		SWI3 VECTOR LSB
FFF2 OR BFF2		SWI3 VECTOR MSB
FFF1 OR BFF1		RESERVED
FFF0 OR BFF0		RESERVED
FFEF-FFE0		NOT USED

LBS: Least significant bit
MSB: Most significant bit

Figure 1-3. Color Computer 2 Memory Map (Cont'd) (PAGE 5)

SECTION II

SPECIFICATIONS

2.1 Physical

Size:	Width – 14.75" (37.5 cm) Depth – 10.35" (26.3 cm) Height – 3.15" (8.0 cm)
Weight:	4.85 lbs (2.2 kg)

2.2 Power:

120VAC 60 Hz, 0.2 Amps RMS typical

2.3 Technical

Microprocessor:		Type – Motorola MC6809E Clock Speed – 0.89 MHz
Memory:	RAM:	16K Expandable to 64K
	ROM:	8K Standard Basic (26-3134) 8K Extended Basic (26-3136), Total of 16K Basic ROM Up to 16K additional ROM (in cartridge)
Keyboard:		53-key microprocessor scanned matrix
Video:		RF Modulated output, channel 3 or 4 32 characters by 16 rows Up to 8 colors Graphic resolution up to 256 x 192 pixels
Sound:	Sources:	Six-bit DAC Single bit Input from cassette recorder Input from cartridge connector
Cassette:		1500 Baud, Frequency Shift Keying
RS232C:		3-wire interface under software control
Joystick:		2 connectors, 2 axes each, DC voltage input of 0.25 to 4.75 volts 64 steps
Expansion:		40-pin cartridge connector containing all major CPU signals necessary for interface.

SECTION III

DISASSEMBLY/ASSEMBLY

3.1 Disassembly

Disassembly of the Color Computer 2 is easily accomplished using only a Phillips screwdriver and a pair of long-nose pliers. Mounting screws for attaching the two halves of the housing are accessible from the underside of the unit. To disassemble the computer, follow the steps noted below.

1. Disconnect power and remove signal cables from the unit.
2. Remove cartridge from slot (if applicable).
3. Turn the unit over and place it on a soft surface to prevent damage to the keyboard or top cover.
4. Loosen and remove the six (two screws (F1) and four screws (F2)) mounting screws which attach the base to the top cover. These screws may not easily come out until the unit is turned over.
6. Disconnect from the PCB the cable which is attached to the keyboard.
7. Tag the three wires from the transformer assembly at the left rear of the unit which are attached to the printed circuit board. Remove the wires using a pair of long-nose pliers.
8. Remove four (two screws (F4) and two screws (F5)) screws which attach the PCB to the bottom case cover. If it is necessary to remove the shield from the PCB do so by removing the seventeen clips ((12)) which attach it to the PCB.
9. Remove the transformer from the unit by removing the two attaching screws. Replacement of the pigtail fuse assembly should be accomplished using the same type and rating fuse.

3.2 Assembly

Assemble the Color Computer 2 in the reverse order of disassembly. The PCB shield is attached to the PCB with metal clips. Five clips ground the shield to the PCB. There are three clips which provide RFI shield ground for the keyboard. These shields must be in place to provide proper RFI shielding.

When reattaching the wires from the transformer to the PCB, ensure that the wires are installed in the slots of the plastic shield between the transformer and the PCB. This will prevent any damage to the wires or insulation when reconnecting the top and bottom covers. Two different types of screws are used to mount the PCB and the top and bottom case parts. Ensure that the correct type is used when reassembling.

The strain relief on the power cord consists of a wrap around the plastic bosses at the rear of the unit. Ensure that the power cord is properly routed to afford strain relief to the transformer connections.

3.3 64K Upgrade Instructions

To upgrade a 16K Memory Unit to a 64K Memory Unit, the following procedure must be followed:

1. Disassemble the unit as noted in Paragraph 3.1 to allow access to the RAM ICs, IC14 through IC21. Remove these eight ICs from the PCB.
2. Install the 64K x 1 ICs (Radio Shack Part No. 8040665 – total of 8 ICs) in place of the ones removed in IC14 through IC21. Ensure that chips are installed as noted with notch in the proper location.
3. Solder a Jumper wire at terminal J1. (See schematic diagram.) J1 is attached to between IC2 and IC7).
4. Run appropriate diagnostic program to verify proper operation of the new memory chips. Assemble the unit in the reverse order of disassembly.

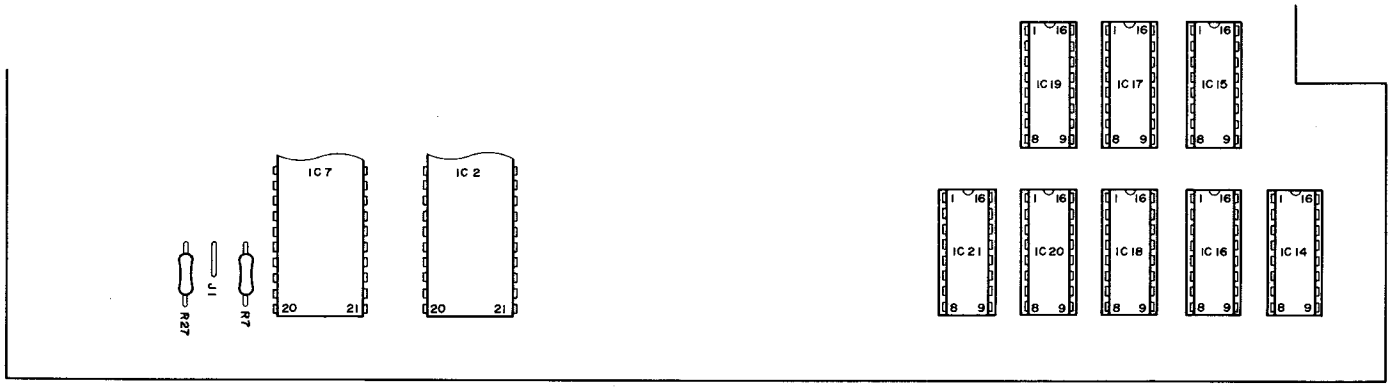


Figure 3-1. 64K Upgrade

SECTION IV

THEORY OF OPERATION

4.1 MC6809E CPU (IC9)

The heart of any computer system is the Central Processing Unit, or CPU. In the Color Computer 2, as well as most modern microcomputers, the CPU is a single Large Scale Integration Circuit (LSI). The CPU gathers instructions and data from memory, interprets and executes the instructions, and stores the results of the data operations into memory. Additionally, the CPU stores data to and retrieves data from various input/output (I/O) devices.

The 6809E Microprocessor is perhaps the most powerful 8-bit microprocessory available today. There are several ways to determine the "size" of a microprocessor (whether it is 8-bit, 16-bit, 32-bit, or whatever). One way involves the number of data interconnecting lines the processor possesses. Another is the size of the internal registers and the size of the mathematical and logical operations supported by the processor. Although the 6809E has an 8-bit data bus, internally it contains four 16-bit registers and two additional 8-bit registers which may be linked together to form another 16-bit register. The 6809E also supports some 16-bit mathematical and logical operations. Therefore, although it is technically an 8-bit processor, it has some of the power of the 16-bit machines.

Figure 4-1 is a "programmer's model" of the 6809E CPU. Following is a brief description of the registers and their respective functions. Additional information may be obtained from the 6809E data sheet.

The Program Counter (PC) register is a 16-bit register. It is the job of the program counter to keep track of which instruction is next. Instructions for the 6809E processor are from one to five bytes in length. As each instruction is fetched, its specific bit pattern allows internal logic in the CPU to determine the length for that instruction. The PC is then immediately updated, even before the remainder of the multibyte instruction is executed.

The Hardware Stack Pointer (S) is another 16-bit register. Its job is to "point" to a specific area of memory that is set aside by the systems programmer for the specific use of the CPU. From time to time, the CPU finds it necessary to "remember" more than it has internal capacity to store. In these cases, it "pushes the data onto the stack." Later, when it is ready to retrieve the information, it "pulls the data from the stack." One example of the use of the stack is the execution of a subroutine. Recall that the program counter has already updated itself to contain the address of the next instruction. The Branch to Subroutine (BSR) instruction will alter the contents of the PC. However, after the execution of the subroutine, the CPU is required to return to the next instruction following the BSR. By storing the return address on the stack prior to the altering of the PC, the CPU is able to return to the main program flow upon encountering the Return from Subroutine (RTS) instruction.

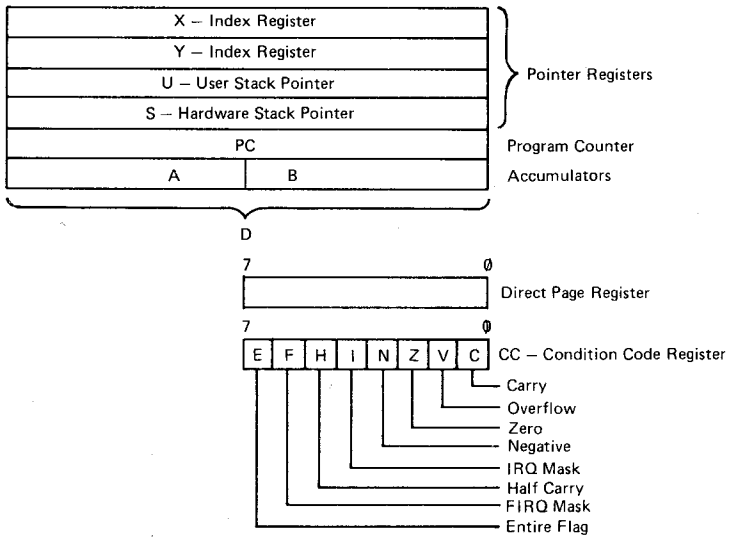


Figure 4-1. MC6809E Programming Model

The S register is also available to the programmer for temporary storage of data via the Push and Pull instructions. In addition, there is a dedicated User Stack Pointer called the U register. This register acts the same as the S as far as the pushing and pulling of data by the programmer, but is not used by the CPU for any of its hardware-related storage requirements.

Two additional 16-bit registers are the X and Y index registers. These registers can be used to mark specific points in memory, such as the beginning of a data table, much the same way a book mark can mark the page that is the beginning of the Logarithmic Tables in the back of a math book. Data can then be retrieved from (or stored into) the table by reference to the pointer used.

The 6809E CPU (IC9) contains two 8-bit accumulators, A and B. The accumulators are the main workhorse registers of a CPU, and are the registers upon which most of the mathematical and logical operations are performed. In the 6809E, the two accumulators can be combined to form one double (D) accumulator, which is then a 16-bit register.

Another 8-bit register is the Direct Page (DP) register. When memory is accessed in the Direct mode, the most significant eight bits of the address will be taken from the DP register.

The Condition Code Register (CC) is best thought of as eight individual bits, rather than an 8-bit group. Six of these individual bits are set or cleared as the result of internal processor operations. The other two bits are used by the programmer to mask out two of the three possible interrupt conditions. The bits are:

C – Carry bit. This bit is set when the result of an operation is greater than the capacity of the register to store it.

V – Overflow bit. Similar to the C bit, but it is set when the result is greater than the capacity of the register to store it in "two's complement" notation.

Z – Zero bit. This bit is set when the result of an operation is equal to zero.

N – Negative bit. The negative bit is set when the most significant bit (sign bit) of an operation is set.

I – IRQ mask bit. The IRQ mask bit is set by the programmer when it is desired to ignore IRQ interrupts.

H – Half-carry bit. This bit is used by the processor in decimal arithmetic operations.

F – FIRQ mask bit. Is set by the programmer when it is desired to ignore FIRQ interrupts.

E – "Entire" flag. This bit is set by NMI and IRQ interrupts, indicating that all registers were preserved. It is cleared by FIRQ interrupts, indicating that only PC and CC were preserved.

Figure 4-2 shows the pinouts of IC9, the 6809E CPU. Note that there are sixteen address lines (A0 through A15). These address lines are output from the CPU and are used to select one of 65,536 different memory locations. The memory and I/O devices must be wired to accept the correct combination of highs and lows on the address lines. The order of the devices and how they respond to the different lines is called the memory map.

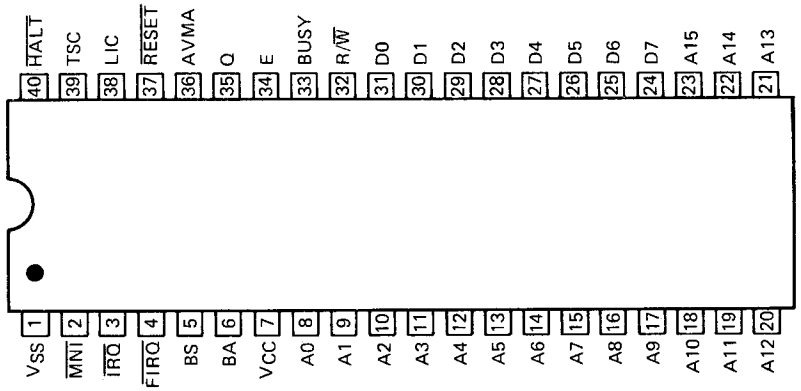


Figure 4-2. MC6809E Pin Assignments

The CPU has eight data lines (D0-D7). These data lines are bidirectional and are used by the processor to both route data to and retrieve data from memory or I/O devices.

The remaining lines on the CPU are used for control functions, both input control and output control. Of course, the Vcc pin is the power input line to the CPU and the GND line is the return reference for both power and signal. The E and Q lines are the clock inputs to the CPU. These clock signals must be present for the CPU to function. In the Color Computer 2, these signals are provided by the SAM chip and are 50% duty cycle clocks at a frequency of 0.89 MHz. As shown in Figure 4-3, Q is a quadrature clock signal which leads E by 90 degrees.

The CPU contains a number of inputs which serve to initiate specific sequences of events. The ones used by the Color Computer 2 are:

RESET* – Used on power up and to reinitialize the CPU.

HALT* – Stops the program flow after the completion of current instruction. Execution will continue after HALT is removed.

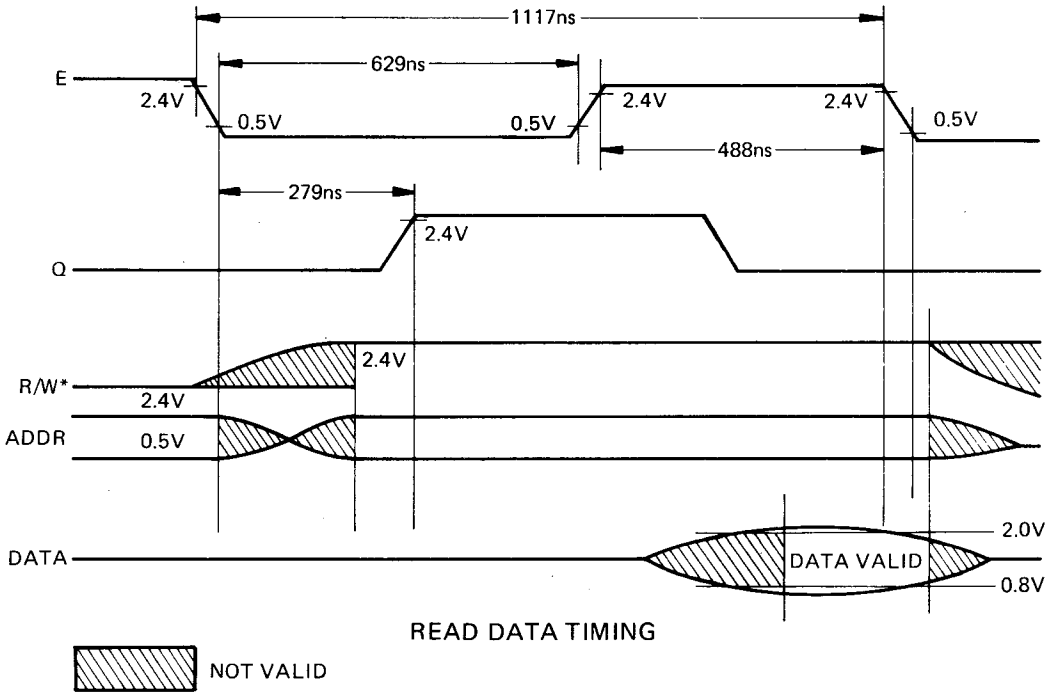
NMI* – Non-Maskable Interrupt. Always causes the CPU to "interrupt" its normal program flow and execute a special "Interrupt handler" routine.

IRQ* – Interrupt Request. Similar to NMI but may be masked (defeated) by setting the I bit in the CC register.

FIRQ* – Fast Interrupt Request. Similar to IRQ, but masked by the F bit. It is faster because it doesn't preserve all registers (as do the other interrupts).

Upon receipt of the RESET signal, or any of the interrupts (if enabled), the CPU will get the appropriate subroutine address from the Vector Table (see the map in the Section I – System Description). For the interrupt routines, registers are preserved on the Stack to be restored upon receipt of the RTI (Return from Interrupt) instruction.

Other control lines used in the Color Computer 2 are TSC (Three-state Control) and the R/W* (Read/$\overline{\text{Write}}$) line. The TSC line is an input intended for use in a multiprocessor or DMA environment and will cause the Address and Data lines to go into a three-state condition if high. Since the Color Computer 2 does not require multiprocessing, this line is permanently grounded. The R/W* line is an output used by the CPU to inform the external memory and devices whether the data transfer is from the CPU (a write) or to the CPU (a read). Standard 6809E Read/Write timing is shown in Figure 4-3. However, in the Color Computer 2, this timing is modified by the SAM chip so that the addresses are presented to the memory only during the active E time. This presents no problem as long as the memory is sufficiently fast.



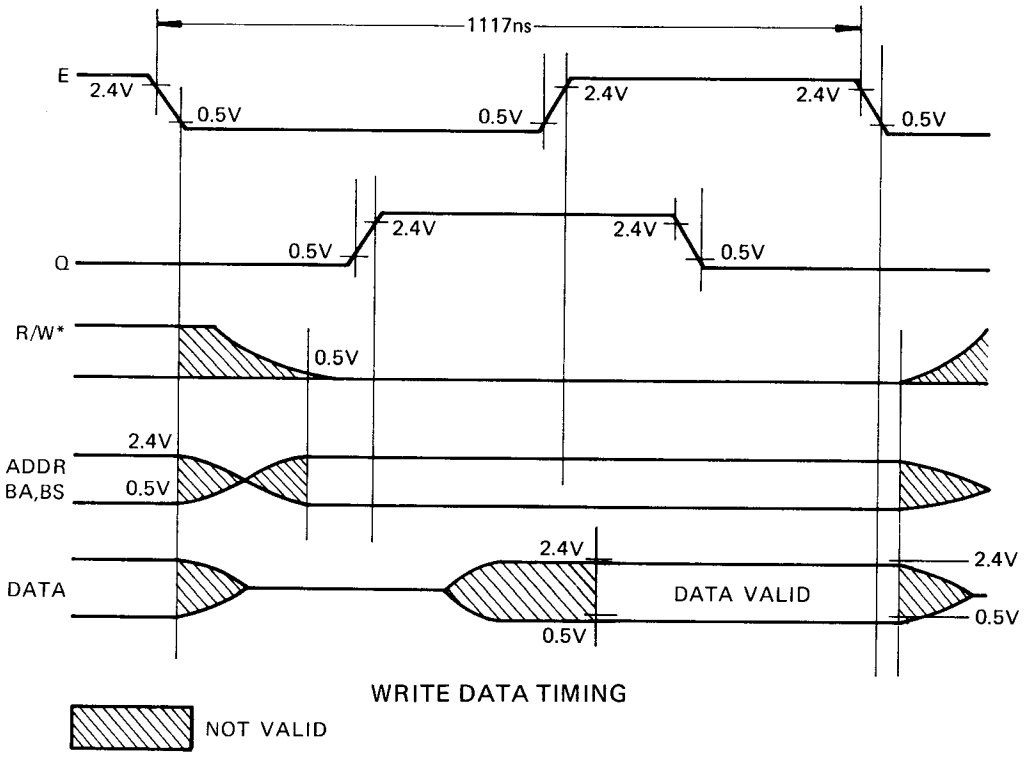


Figure 4-3. MC 6809E Read/Writing Timing at 0.89 MHz.

4.2 Reset Circuit

The reset circuit is comprised of R20, R22, C48, C58, D10, D11, and D12. This circuit provides pulses of two different time durations for power-up or reset. R22 and C58 provide a pulse of approximately 10 milliseconds which is used to reset the SAM chip (IC22). The reset input to IC22 is also used as an output, so diode D10 is used to isolate the output signal from pin 7 of IC22 from the rest of the reset circuitry.

The second reset pulse is the master system reset signal. This is provided to the CPU and both PIA's (IC2 and IC7). C48 and R20 provide this master reset pulse of approximately 100 milliseconds. D11 is used to isolate the two R/C circuits. D12 becomes forward biased upon power down and is used to discharge capacitors C48 and C58, rather than them having to discharge slowly through their normal charging resistors (R20 and R22).

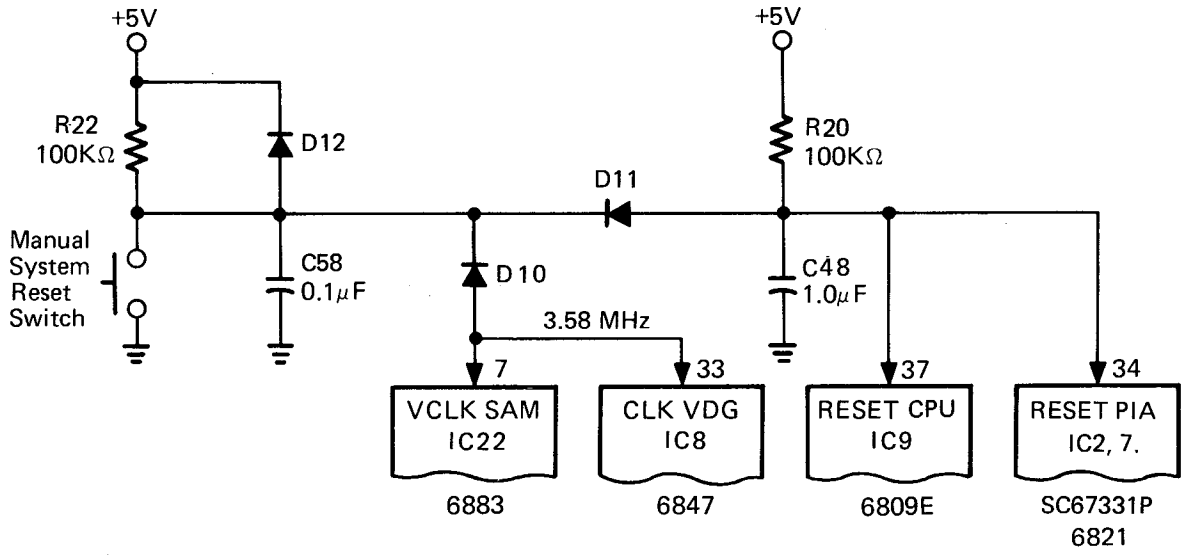


Figure 4-4. MC 6883 Reset Circuitry

4.3 Memory

The Color Computer 2 uses Dynamic Random Access Memories (DRAMs, IC14 thru IC21). Each memory chip is capable of storing 16,384 bits (16K), any one of which may be accessed at any given time. Since the CPU needs to access eight data bits at a time, eight DRAMs are used. Therefore, the memory array is said to be 16K x 8. The DRAMs in the Color Computer 2 operate from a single +5 volt supply.

In order to address 16K locations in each chip, 14 address lines are required. However, since the DRAM package has only 16 pins, the addresses are multiplexed into two groups of 7, called row address and column address. See Figure 4-5. The row address is presented first, and the DRAM is informed that this is the row address by the presence of RAS* (row address strobe) and the absence of CAS* (column address strobe). After the DRAM has latched the least significant seven addresses (the row addresses), the column addresses are presented, along with CAS*. If the present cycle is a read cycle, WE* (Write Enable) is held high, and the data is retrieved from the appropriate cell and presented at the output pin some time later. The actual time depends on the access time of the DRAM. During a write cycle, the data and WE* signal are active prior to CAS and are latched in at CAS time. Figure 4-6 shows the read and write timing cycles for DRAM.

Dynamic memory is called dynamic because it requires refreshing at periodic intervals in order to remember. Refresh is accomplished by providing the DRAMs with the RAS signal and an address count. The address count must toggle through all 128 possibilities in 2 milliseconds or less. (If you don't remind the DRAM of what it knew every 2 milliseconds it will forget, which is not very good for memories.)

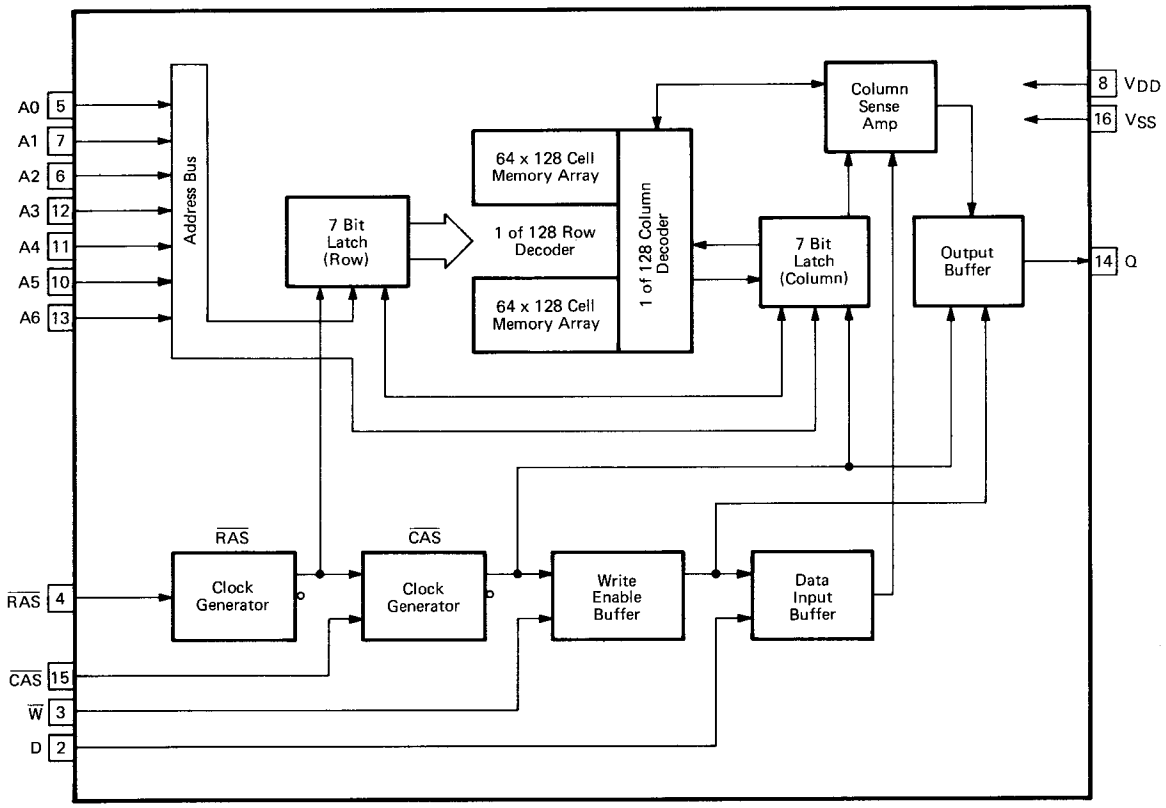


Figure 4-5. DRAM Block Diagram

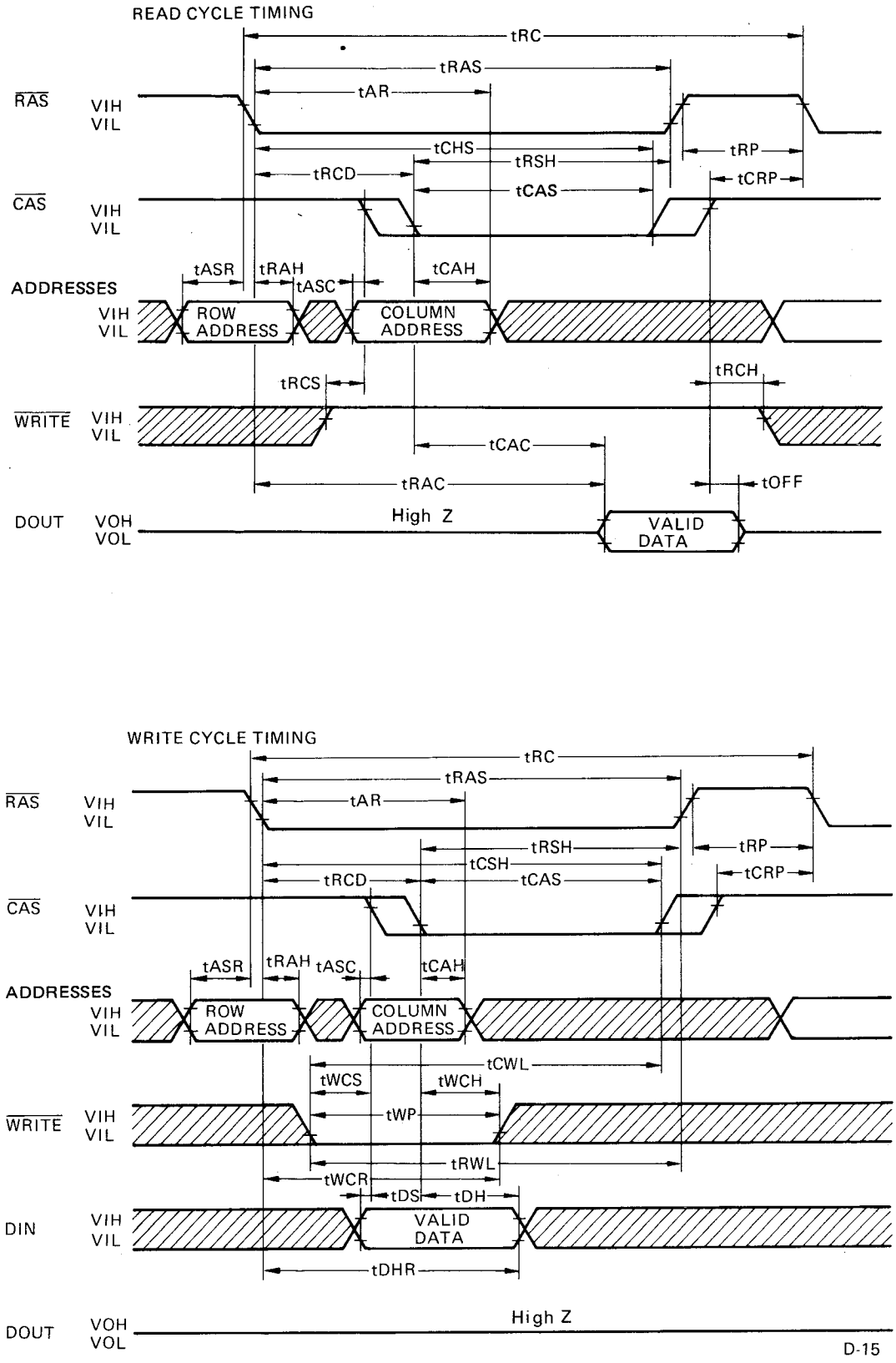


Figure 4-6. DRAM Timing

By now, it should be apparent that controlling DRAMs is a fairly complex task. In the Color Computer 2, it is done by the 6883 Synchronous Address Multiplexer (SAM, IC22) chip. In addition to address multiplexing, RAS* and CAS* generation, WE* timing control, and refresh generation, the SAM performs other tasks. It contains the Master Oscillator, the frequency of which is controlled by a 14.31818 MHz crystal (X1). The Master Oscillator is divided by four to give a 3.579545 MHz color reference signal to the Video Display Generator (VDG, IC8) chip and to the chroma/RF modulator. This signal is then divided by four again to produce the 0.89 MHz E and Q signals which are required by the processor (IC9).

The SAM chip (IC22) also controls access to the memory, granting access to the processor during the high time of E and access to the VDG chip during the low time of E. During each access, whether by the CPU or the VDG, the SAM must provide appropriately synchronized RAS* and CAS* signals, as well as the corresponding address signals, to the DRAMs. Note that the DRAM access time must be twice as fast as that required by the CPU alone in order to be able to respond to VDG accesses. The Color Computer 2 uses 200 nanosecond access DRAMs.

In order for the SAM chip to provide the appropriate addresses to the DRAMs, all 16 CPU address lines are input to the SAM. It then multiplexes these into low order and high order addresses (Z0 through Z7) which it sends to the DRAMS along with RAS* and CAS*. During a VDG access, the SAM must also "know" the current display address put out by the VDG. In order to accomplish this with a minimum pin count on the SAM, the dividing chain internal to the VDG is duplicated in the SAM. The count is reset upon receipt of FS* from the VDG and is advanced by subsequent occurrences of DA0. It is necessary for the SAM to duplicate the exact display mode of the VDG in order for the addresses to come out right. For this reason, the SAM contains some programmable registers (see the Memory Map, Section I).

The final function of the SAM is to provide address decoding and device selection for the computer. Figure 4-7 shows how the S0, S1, and S2 lines are connected to IC11, a 74LS138, in order to provide appropriate signals to enable RAM reading, ROM selection, PIA selection, and various cartridge selection signals. Due to the nature of the ROMs and in order to prevent data bus contention, the ROMs are enabled only during the E portion of a read cycle. This is accomplished by the 74LS02 NOR gate, IC10.

Additional details of the SAM chip may be obtained by referring to the 6883 data sheet.

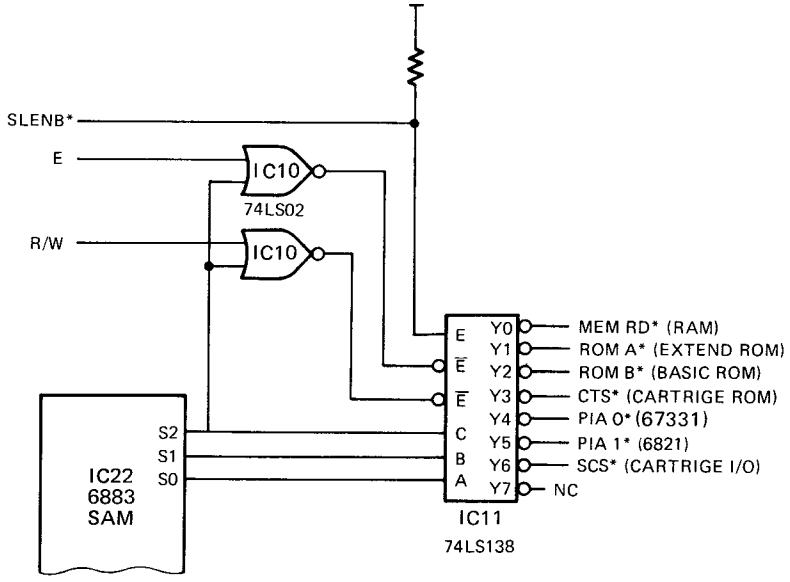


Figure 4-7. Color Computer 2 Address Decoding

4.4 Video Generation Circuitry (IC8)

A computer without some method of providing output to the user would not be of much value. In the Color Computer 2, the main method of providing output is via the RF modulator which provides a composite chroma signal into a standard color (or black and white) television. However, most of the modulator's job is to translate computer-like signals into signals the television can use. The portion of the Color Computer 2 that actually generates the computer-like video signals is IC8, the 6847 Video Display Generator, or VDG chip.

A television set displays images by sweeping an electron beam across the face of the screen very rapidly from left to right, and somewhat more slowly from top to bottom. The electron beam strikes the phosphorescent surface on the screen causing it to glow. If the intensity of the beam is reduced, the screen is less bright. If the intensity is increased, the screen glows brighter. The screen is actually coated with three different color phosphors (red, blue, and green) and, by combining the intensities of each, different colors are produced.

The VDG chip produces the signal which eventually controls the intensity of the sweeping beam. This is the "Y" signal which also contains vertical and horizontal synchronizing pulses to ensure that the television begins each line or frame at the correct time. Additional signals from the VDG chip which serve to determine the color displayed on the screen are ϕA, ϕB, and CHB. Without these three signals, the television would produce only a black and white picture.

As stated before, the Y signal determines the intensity of the light produced by the television. In order to produce a desired character, the Y signal must turn the beam on only at the desired times. As the beam sweeps from left to right for the first time in each frame, the top portion of each character in the row is displayed, and so on. The beam sweeps an entire frame of 192 lines in one sixtieth of a second before beginning over. The high repetition rate, as well as the persistence of the phosphor, causes the human eye to perceive the screen display as a whole.

In order for the Y signal to produce the same screen on successive frames, it must get the information from somewhere. In the Color Computer 2 the information is stored in the DRAM.

The VDG has an address generation scheme (which is duplicated in the SAM) that enables it to determine where in memory the data is stored for a particular area (character cell) of the screen. During the low portion of the E cycle, the CPU is not using the bus, so the VDG (actually the SAM) puts the address for the next character on the address bus. The data is then latched into IC5, a 74LS273, by the rising edge of the RAS* signal. This ensures that the data will be stable at the VDG data inputs, even if the CPU has started its next memory access by the time the VDG is ready to receive the data.

In the alphanumeric mode, the data retrieved from the DRAMs by the VDG is in the form of ASCII character codes. This data is then used by the VDG's internal character generator, along with the "line count" information, which is kept track of internally, to decide which dots to display. The dot data is loaded into two internal shift registers which are clocked on alternate polarities of the incoming 3.58 MHz clock. The outputs of these shift registers, along with the vertical and horizontal sync signals, become the Y signal. In the graphics modes of operations, the data retrieved by the VDG contains actual pixel and color information, and is used to generate the ϕA and ϕB signals in addition to the Y signal. The CHB signal is a chroma reference signal and is used to compensate for temperature drift and other anomalies.

The GM0, GM1, GM2, A/S, A/G, INT, and CSS lines are used to determine the display mode of the VDG. These are controlled by one of the output ports on PIA IC2. For more information, refer to the memory map and the VDG data sheet. The HS* output of IC8, the MC6847, occurs during horizontal sync time and is used as one possible source of interrupt to PIA IC7. The FS* output occurs during vertical sync time, and is used as another possible (60 Hz) interrupt source to PIA IC7. In addition, the FS* output is tied to the MS* input of the VDG, disabling the address bus after the active display time and allowing the SAM chip to supply refreshing for the DRAMs.

The Y, Phase A, Phase B, and CHB signals from the VDG, as well as the Sound signal and the 3.58 MHz chroma clock, are sent to the RF modulator. The heart of the modulator is the MC1372 integrated circuit which takes these inputs (except for the sound) and modulates an RF carrier with them. The sound input is used to frequency modulate a 4.5 MHz sound carrier oscillator contained in the modulator. This modulated sound signal then enters the MC1372 with the chroma information, thus modulating the RF carrier.

The modulator should be considered a sealed unit and, if defective, replaced as a unit. No attempt should be made to repair the modulator.

4.5 Artifacting

The Motorola MC6847/MC1372 component combination is designed to produce several modes of graphics operation. The highest resolution mode (192 by 256 pixels) is designed to be a black and white mode. In this mode, the MC6847/MC1372 component combination does not produce the color burst signal necessary to make the television "see" color.

Artifacting is a phenomenon whereby a color television set can reproduce color from essentially a black and white signal, if the period of the signal is less than that of the color oscillator signal. However, for the television set to do this, it must receive the color burst signal.

The artifacting circuit in the Color Computer 2 forces the Motorola MC1372 to generate the burst signal in the high resolution mode, contrary to the original design of the component. In addition, the phase of burst generated is controlled to a limited degree in order to produce a desired set of hues, or tints, from the black and white signal which is now being interpreted as color.

The Color Burst signal is approximately eight cycles of 3.58 MHz riding on the back porch of the horizontal sync pedestal. In the television, this signal is used to synchronize the set's internal chroma oscillator in both frequency and phase to the transmitted signal, so that the proper colors are demodulated. The phase of the chroma signals with reference to this signal determines the tints of the colors on the screen.

Additionally, the absence of this burst signal triggers a "color killer" circuit in the TV set, which shuts off the chroma bandpass amplifiers in the set. The purpose of this is so that old black and white programs will be seen without colored "snow", which is random noise amplified by the chroma bandpass amplifiers. With no burst received by the TV, the color killer should insure that the set produces a black and white picture.

The colors produced in the artifacting mode depend upon the phase of the signal that is being interpreted by the TV as burst. It is possible to force the MC6847 (IC8) into one of the color modes during horizontal sync time and thereby cause it to send the signal to the MC1372 which makes it generate burst, returning to the correct mode before the display is active. However, if this approach is used, the burst generated by the MC1372 will cause the TV to reproduce the "free colors" as magenta and green, which is not acceptable.

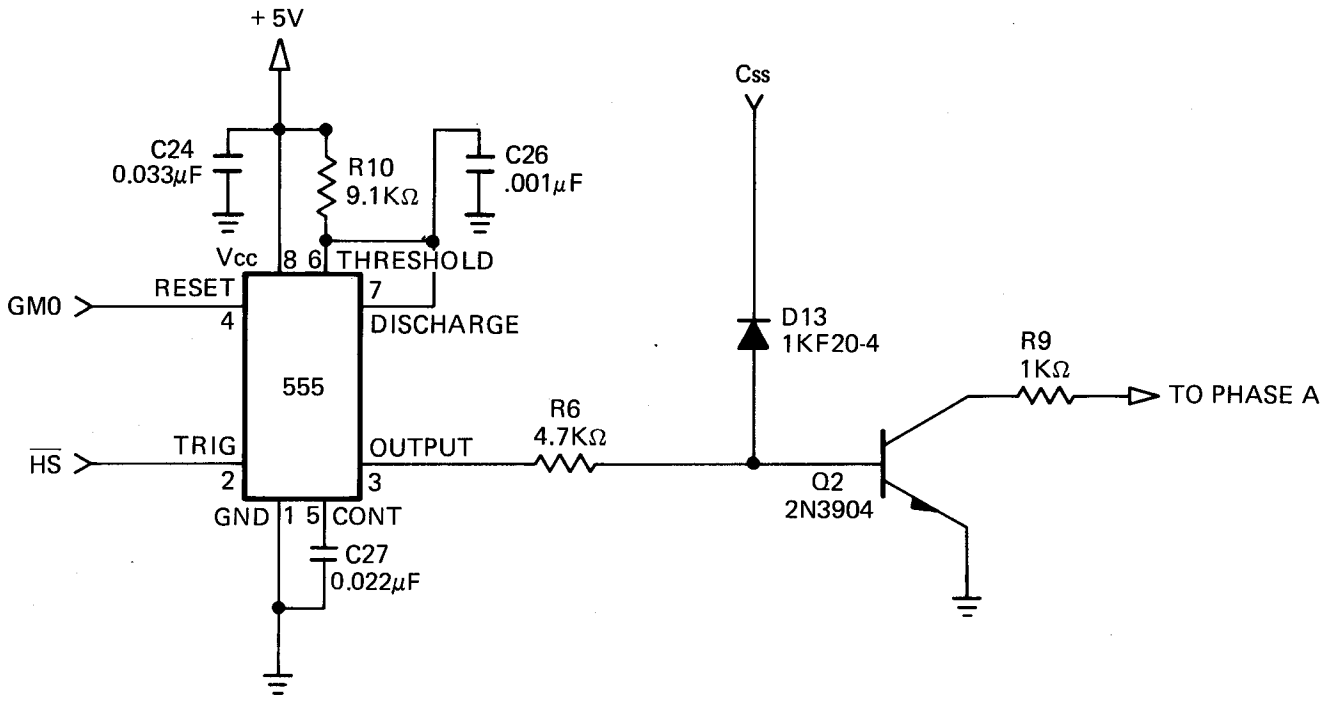


Figure 4-8. Color Computer 2 Artifacting Circuitry

The apparent problem at this point is how to get the MC1372 to produce a phase of the burst signal which will produce red and blue. The MC1372 has two "color phase" inputs, Phase A and Phase B. Essentially, these are inputs to balanced modulators, each of which is referenced to a Chroma Bias signal. The other input to each balanced modulator is a phase of the 3.58 MHz clock, with Phase A lagging Phase B by about 100 degrees. This allows amplitude changes on Phase A and Phase B inputs to determine the tint of the composite chroma output. The way the MC6847 causes the MC1372 to generate burst is by unbalancing the Phase B input in a negative direction during back porch time. However, unbalancing Phase A in a negative direction produces the desired colors.

It is important that the unbalancing of this signal be accomplished during back porch time and that the Phase A signal be allowed to return to it's normal (steady) level before the active video time for the scan. The circuit in Figure 4-8 accomplishes this. If GM0 is high, then the horizontal sync pulse is allowed to trigger the one-shot. This turns on the transistor (Q2) for a duration of about 10 microseconds, provided the diode (D13) is reverse biased (which it will be if CSS is high). When the transistor conducts, it will unbalance the Phase A input to the MC1372 in the negative direction, causing it to generate burst. Note that both GM0 and CSS must be high in order to force any change in the input signal to Phase A. This occurs when in the high res mode. At all other times, the transistor is off, its leakage is negligible, and hence R9 is essentially connected to nothing.

4.6 PIAs (IC2 and IC7)

The Color Computer 2 uses two Peripheral Interface Adapters (PIAs). These devices provide a universal interface to the 6809E CPU. They support all of the I/O functions in the Color Computer 2.

The functional configuration of the PIA is programmed by the CPU during the reset routine. Each of the peripheral data lines may be programmed to act as an input or output, and each of four control/interrupt lines may be programmed for one of several control modes. Figure 4-9 shows a block diagram of a PIA.

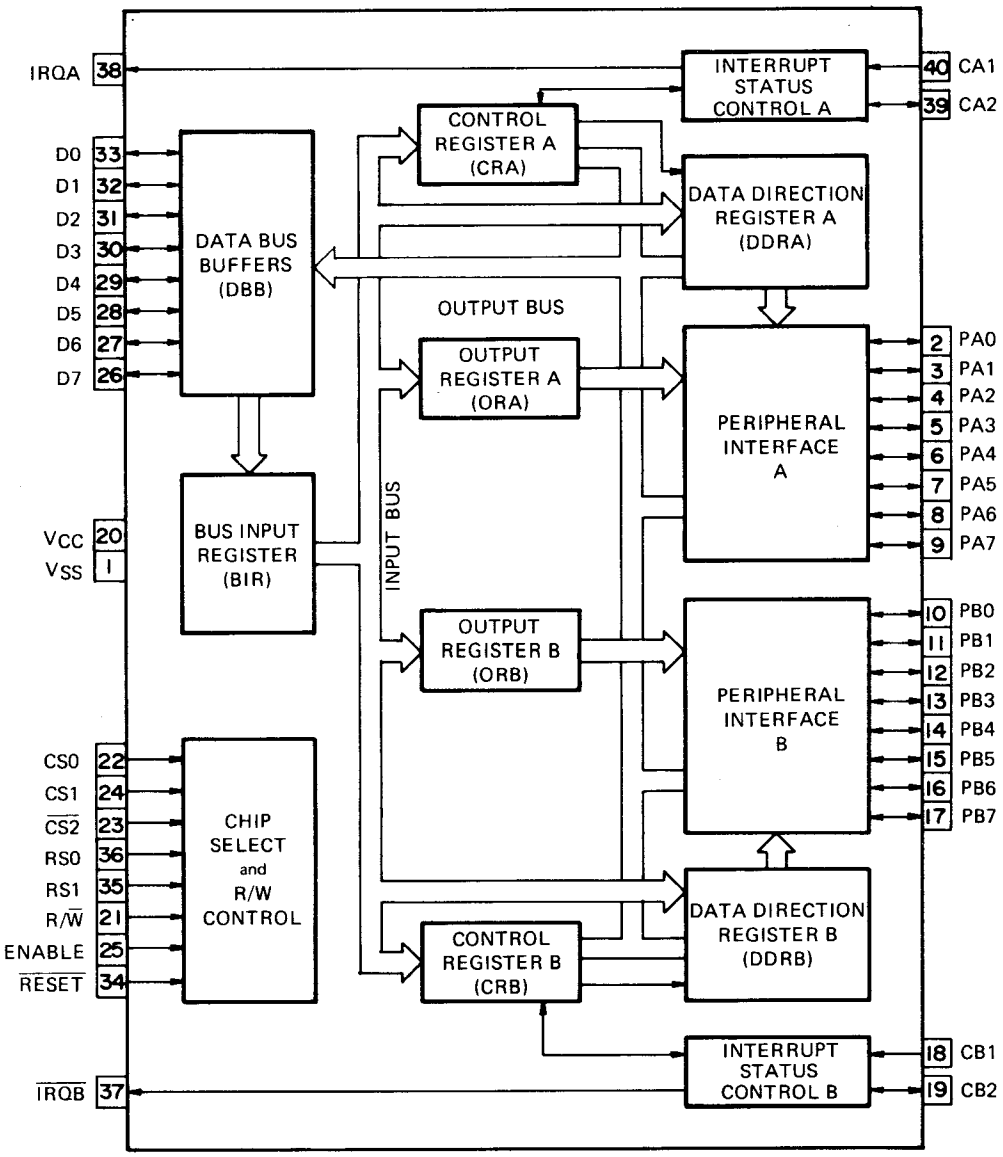


Figure 4-9. PIA Block Diagram
MC 6821P
SC67331P (6821 Select)

As shown in Figure 4-9, a PIA consists of two 8-bit data registers and 4 control/interrupt lines. The two 8-bit data registers are controlled by two data direction registers. These direction control registers are set up by the reset routine and normally will not be changed.

The four control/interrupt lines are controlled by the two control registers. The control registers also handle device selection within the PIA. Two of the four lines function only as interrupt inputs, and the other two lines may be used as interrupt inputs or outputs.

PIA IC7 is used mainly for the keyboard. Data register B (pins 10-17) is programmed as an output and is used to strobe the keyboard columns. The first seven lines of data register A (pins 2-8) are programmed as inputs and are used to read the keyboard rows. Pins 2 and 3 are also used as fire button inputs for the joysticks.

The other pins of PIA IC7 serve various functions. The most significant bit of data register A (pin 9) is programmed as an input for the joystick interface. CA2 and CB2 (pins 19 and 39) are used as outputs. These two lines select one of four joystick or sound inputs. The last two pins of PIA IC7, CA1 (pin 40) and CB1 (pin 18), are used interrupt inputs. They are both tied to video clock outputs from the VDG (IC8). If enabled, CA1 provides an interrupt after each video line. CB1, if enabled, provides an interrupt after each screen of data (60 Hz).

PIA IC2 is used for several different functions. Pins 4-9 of data register A are used for the 6-bit digital to analog converter. Pin 3 of register A is the RS-232C output signal, which is used to drive the printer and other RS-232C-type devices. Pin 2 of register A is the input for data from the cassette. Pins 13-17 of data register B are used to control the selection of the various alphanumeric and graphic modes of the VDG. Pin 12 of register B is an input for the memory size jumper. Pin 11 of register B is the single bit sound output. Pin 10 is the RS-232C signal input pin.

The control and interrupt pins of PIA IC2 also serve various functions. CA1 (pin 40) is the input for the signal CD (a status interrupt input for the RS-232C interface). CA2 is an output used to control the cassette motor. CB1 is the cartridge interrupt input. Whenever a cartridge is inserted into the computer, this input will interrupt BASIC and jump to the program in the cartridge. Finally, CB2 is used as an output to enable sound from the DAC chip (IC3).

4.7 ROM (IC12 and IC13)

ROM stands for Read Only Memory, which is a type of memory that retains its data when power is removed from it. When power is applied to the CPU, it immediately attempts to fetch a vector and begin executing instructions. If there were no ROM, the CPU would read random floating states on the data bus, attempt to execute this, and promptly go haywire. The Color Computer 2 contains either one or two ROMs, depending upon whether it is Standard or Extended Color BASIC. Each ROM contains 8K bytes which are programmed to provide the user with certain BASIC commands and functions. IC12 contains Standard BASIC, and IC13 is the socket for the Extended BASIC ROM. IC12 must always be installed, even in the Extended BASIC machine. Note that all address and data lines, as well as Vcc and ground, are paralleled to the two ROMs. The only line that is independent for each ROM is the CE or chip enable line which is provided by IC11, the 74LS138, as appropriate.

4.8 Keyboard Interface (IC7)

PIA IC7 is the only active component in the keyboard interface circuit. The B side of this PIA is configured as outputs, and connects to the column lines of the keyboard matrix. The A side of IC7 is configured as inputs, and connects to the row lines of the keyboard matrix. PIA IC7 is a select device. The use of PIA compensates for a possible increase in key contact resistance due to prolonged use, and therefore should result in a highly reliable keyboard interface.

To read the keyboard, only one column is enabled by writing a zero in the bit that corresponds to that column and by writing ones in all the other bits. If a key is being pressed in that column, one of the input lines will be a zero and the key location will correspond to the bit that is low. By scanning each column in the keyboard, all of the keys may be checked. Figure 4-10 shows the keyboard matrix.

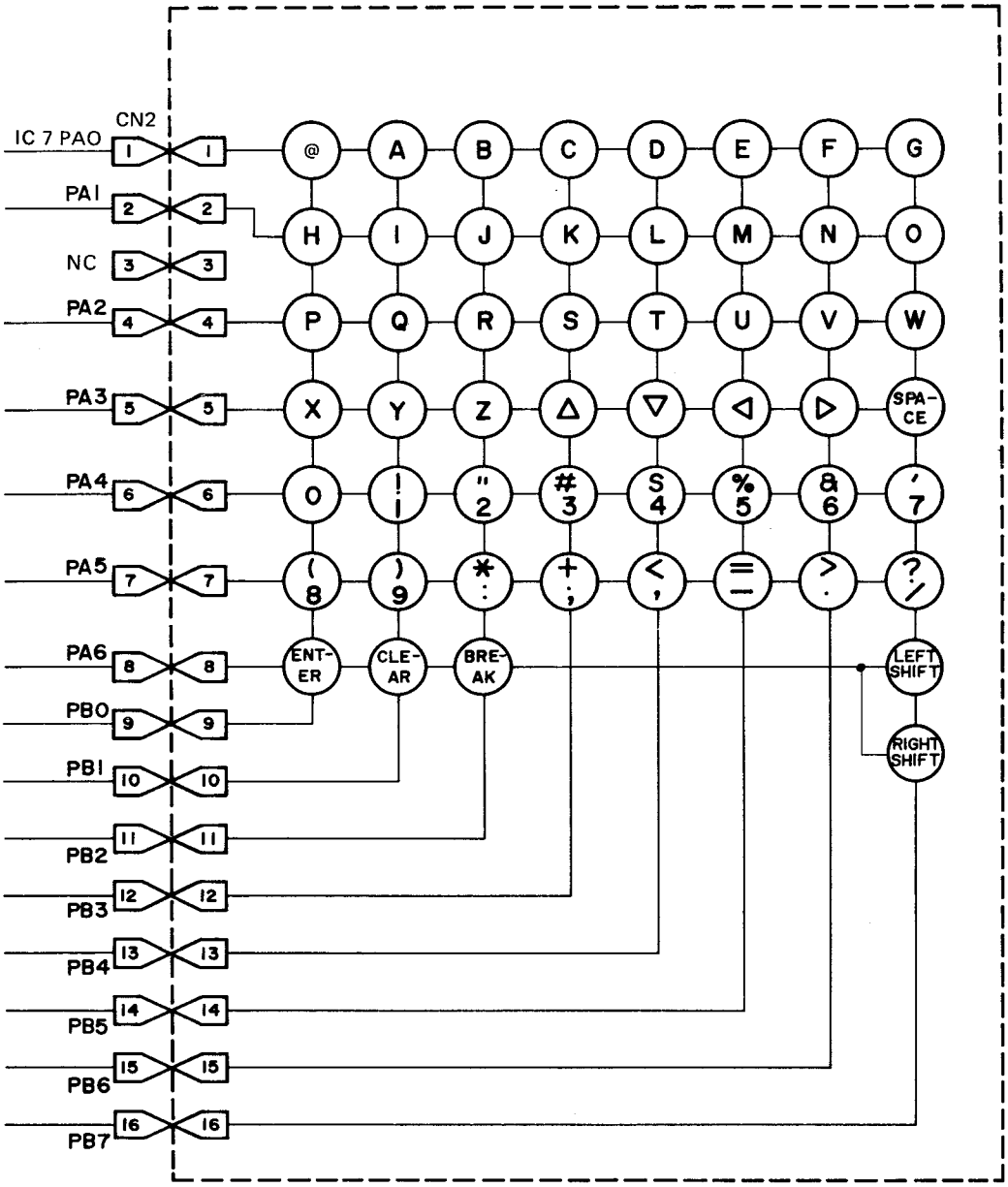


Figure 4-10. Color Computer 2 Keyboard Array

4.9 DAC Circuitry (IC3)

Two special analog integrated circuits are used in the Color Computer 2 to implement a multitude of analog functions including power supply regulation, cassette operation, the RS-232C serial interface, the joystick interface, and sound production/selection. The DAC chip (IC3) is one of the custom linear integrated circuits used in the Color Computer 2. As its name implies, it contains a Digital to Analog Converter. This chip also contains a sound multiplexer and the circuitry necessary to interface the joystick controllers to the microprocessor. Figure 4-11 shows a block diagram of the DAC chip.

The DAC itself performs most of the functions of this chip. Six bits of control are used by the DAC to specify a discrete internal analog level. This level is one of the sound inputs to the sound multiplexer. It is also used as a reference for a comparator, the other input of which is one of the four joystick inputs. Finally, the DAC signal is attenuated and used as the cassette recording signal for data storage.

There are two select inputs to the DAC chip: Sel A and Sel B. These determine which of the joystick inputs is to be compared against the DAC, as well as which sound source is coupled to the sound output pin according to the following table:

Sel B	Sel A	Joystick Input	Sound Source
0	0	Joy 0	DAC
0	1	Joy 1	Cassette
1	0	Joy 2	Cartridge
1	1	Joy 3	(no sound)

The Digital to Analog Converter employs a 64-collector transistor as a current source which gives good linearity over the entire voltage range. In order to determine the position of the joystick, the microprocessor uses a technique called "Successive Approximation". The microprocessor first selects the desired joystick input by means of the select pins (which are connected to PIA IC7).

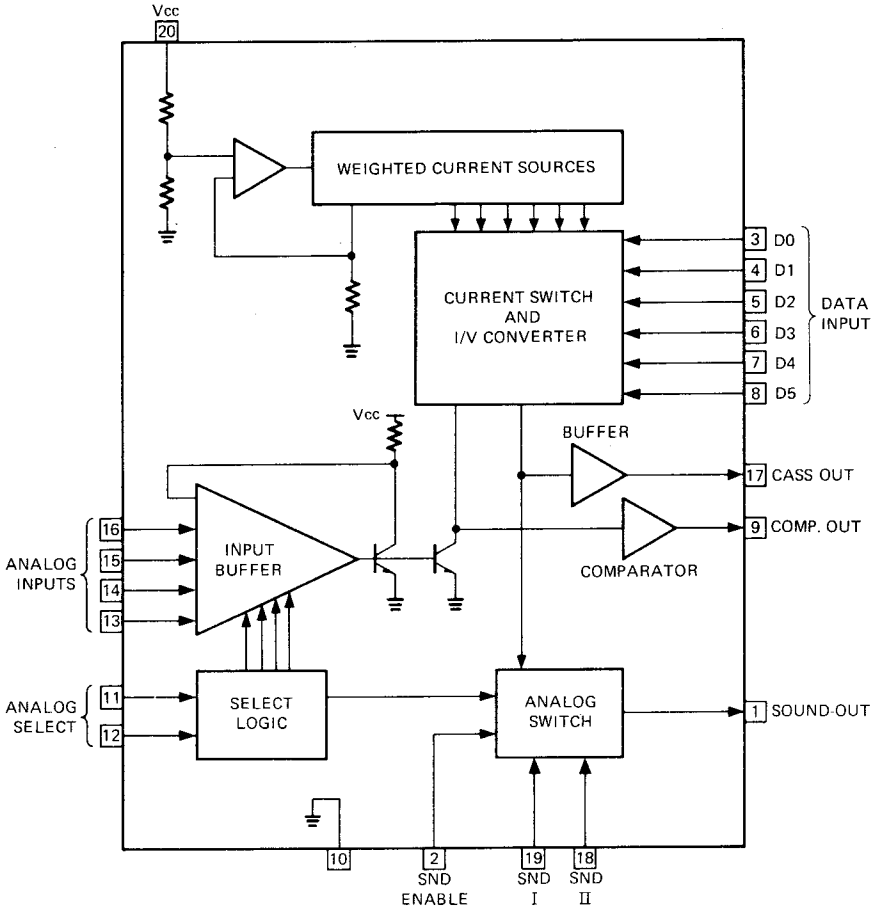


Figure 4-11. DAC Block Diagram

Next, a value equivalent to the midpoint of the voltage range, 32 decimal for example, is sent to the DAC's six bit input via PIA IC2. If the DAC output voltage is lower than the joystick voltage, the HI/LO pin of the DAC chip (comparator output) is low. However, if the DAC voltage is higher, the HI/LO pin is high (logic one). If the HI/LO pin was low, the next value the microprocessor tries is half-way between 0 and the last value, or 16 decimal. If the HI/LO pin was high, the microprocessor tries a value half-way between the last value and 64, or 48 decimal. For each value, the microprocessor either adds or subtracts half the value of the preceding difference, until the final value is found. Since the DAC uses six binary digits, exactly six DAC settings are required to determine the "position" along one axis of the joystick. The four joystick inputs to the DAC chip correspond to two axes for each of two joystick controllers.

The sound multiplexing section is very simple. According to the above table, different sound sources are selected by the Sel A and Sel B inputs, and the selected input is routed to the sound output. If the DAC is used as a sound source, the microprocessor simply feeds a succession of values to the six bits of the DAC in order to produce the desired waveshape. The output of the DAC is then buffered and attenuated to provide approximately 3.9 volts p-p, which is the level required by the modulator to produce maximum volume. If the cassette is the selected input, then sound from the cassette recorder is routed to the sound output. This level follows the input level up to 3.9 volts p-p, at which point it clips the input waveform. Therefore, the volume control on the cassette should not be set higher than the level which provides 3.9 volts p-p to the DAC chip. Similarly, the cartridge may supply the sound source (from AC coupled) since the SND input to the DAC chip biases the input at the midpoint of the allowable voltage swing, which is 3.9 volts p-p. Any greater signal amplitude will result in clipping (distortion) of the sound waveform.

In addition to the Select inputs, the sound must be enabled by bringing SNDEN to a high level. This input is controlled by PIA IC2. If this pin is at a low level, all sound (except single bit sound) is disabled.

The final function of the DAC chip is to provide the output signal for recording of cassette data. This is, quite simply, a buffered output of the DAC which is attenuated to produce approximately 1 volt p-p into a 2K ohm load. Therefore, it is up to the microprocessor to produce the necessary FSK signals through the DAC and the proper software.

4.10 SALT Circuitry

The SALT chip IC1 (Supply and Level Translator) is responsible for supply regulation, RS-232C interface level translation, cassette read operations, and driving the cassette relay, as is shown in the block diagram is Figure 4-12.

Figure 4-16 shows the complete power supply circuit. AC voltage is brought into the primary of transformer T1. The secondary of the power transformer provides 17.2 VAC, center-tapped, at 1.8 amps RMS to the Color Computer 2 circuit board. If switch SW1 is closed, this AC voltage is applied to the cathodes of D1 and D2, and to the anodes of D3 and D4. D1 and D2 form a full wave center tapped rectifier with a negative output. This is filtered by electrolytic capacitor C1. This negative voltage is then applied to pin 15 of the SALT chip, where it is internally regulated to -5 VDC and used for the RS-232C output drivers. The negative voltage is not used anywhere else in the computer.

D3 and D4 form a full wave center-tapped rectifier with a positive output which is filtered by electrolytic capacitor C2. This positive voltage is applied to the collector of pass transistor Q1 and is used to power the SALT chip at pin 16. The SALT chip internally regulates the positive voltage to +5 VDC and provides the base drive current for Q1. The current for the computer is drawn from the emitter of Q1 through resistor R2. The voltage at this point is monitored by pin 3 of the SALT chip and the base drive adjusted to keep the voltage at a steady +5 VDC, +/- 5%. Electrolytic capacitors C5 and C11 are used to prevent oscillation of the power supply.

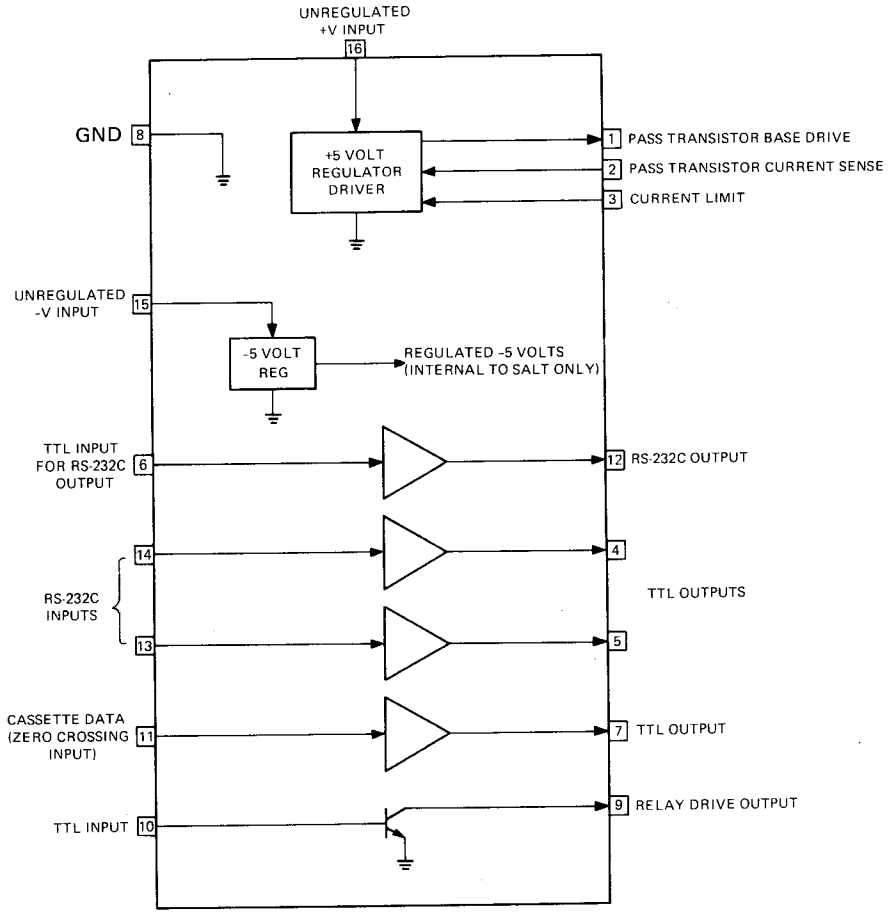


Figure 4-12. SALT Block Diagram

The SALT chip senses, at pin 2, the amount of current drawn from the supply through R1. If excessive current is drawn, as in the case of a short or component failure, the SALT will "fold back" the voltage output of the supply by reducing the base drive current, thus protecting the supply.

Inductors FB1 and FB2, as well as capacitors C7 through C4, serve to decouple and prevent any digital "noise" which might be present on the DC supply from entering the AC line.

There are two types of Level Translators contained in the SALT chip for use with the RS-232C interface. The output level converter takes as its input a standard TTL signal from PIA IC2, inverts it, and uses it to drive the output to approximately +5 VDC for a space and -5 VDC for a mark. This output is coupled through a 270 ohm resistor, R3, to the output connector. R3 serves to limit the amount of current drawn from this output and prevent damage to the SALT chip if the output (at the connector) is inadvertently shorted to an external voltage (such as ±12 VDC, which may be present on some RS-232C connectors).

The input level converters have the task of converting incoming RS-232C voltage levels to standard TTL signals. These voltages are defined as follows: a "mark" is a negative voltage between -3 and -25 VDC; a "space" is a positive voltage between +3 and +25 VDC. To simplify the task for the SALT chip, the circuit shown in Figure 4-14 (resistor/zener diode combination) is employed. D5 and D6 clamp the negative voltages and prevent them from reaching the SALT chip. The incoming signals are compared to a reference of 2.0 VDC. If less than that, they are considered to be a mark. If greater than that, they are considered a space. The space or mark is then output from the SALT chip at an LS TTL compatible level, and is coupled into PIA IC2.

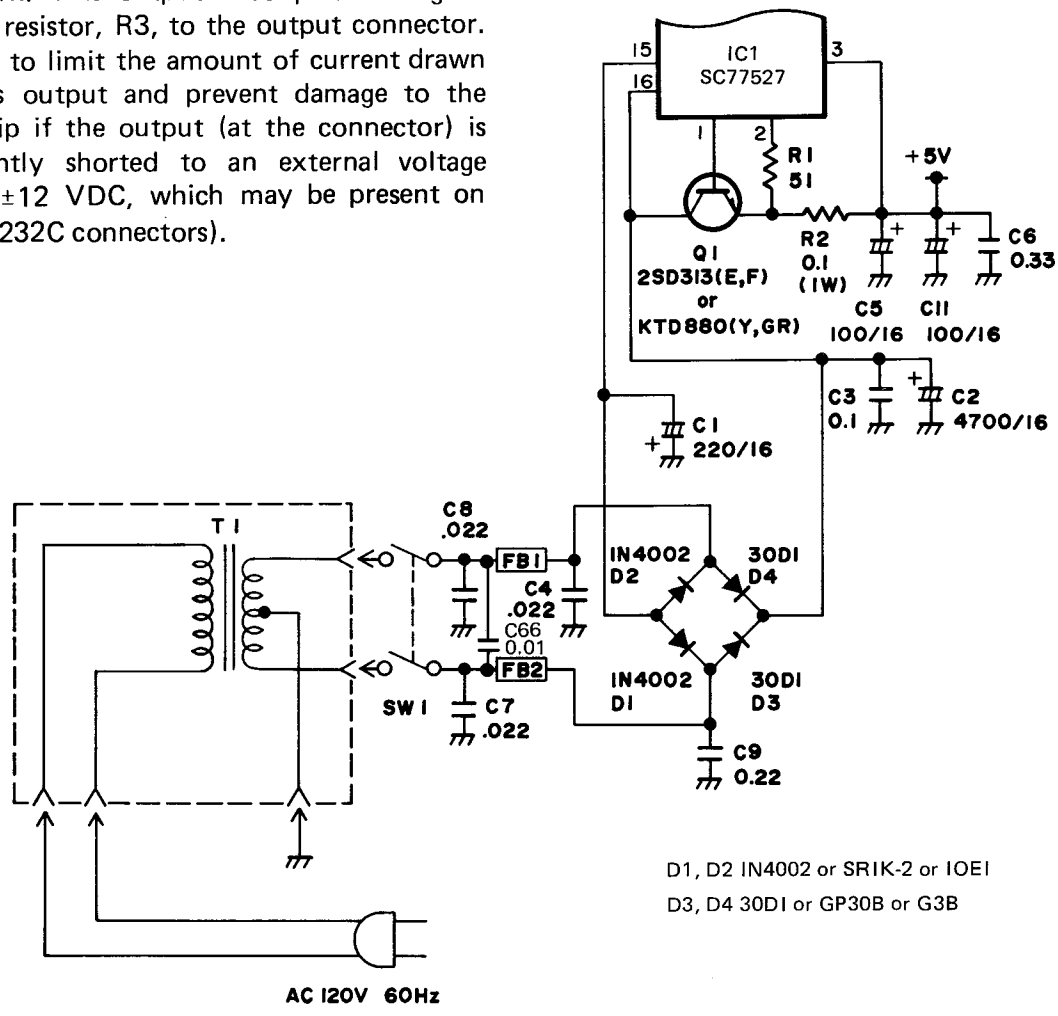


Figure 4-13. Color Computer 2 Power Supply

The cassette loading circuitry internal to the SALT chip is composed of a zero crossing detector. Figure 4-14 shows the input from the cassette being loaded by a 220-ohm resistor, R23, then coupled into the SALT chip through a 510-ohm resistor, R4. R23 serves to load the capacitively-coupled output characteristic of most portable cassette recorders, and R4 limits the current of the incoming signal to prevent damage to the SALT chip if an excessively large peak-to-peak voltage is fed into the cassette input. Although Radio Shack's CCR-81 does not produce more than 6 volts p-p, the circuitry is protected from voltages as high as 18 volts p-p. The zero-crossing detector internal to the SALT changes state each time the incoming signal passes through zero volts. There is a small amount of hysteresis built in which provides noise immunity and prevents false triggering of the zero-crossing detector. The output of the zero crossing detector is an LS TTL compatible level and is coupled into PIA IC2.

The final function of the SALT chip is to drive the cassette relay. A TTL signal from PIA IC2 enters pin 10 of the SALT chip where it is connected to the base of an internal Darlington transistor, the emitter of which is grounded. The collector exits the SALT chip at pin 9, and is connected to one end of the cassette relay. The other end of the relay connects to +5. When the incoming signal goes high, the transistor becomes saturated and connects its end of the cassette relay to ground, causing the relay to energize. When the incoming signal is low, the transistor is cut off. There is no ground return for the +5 volts at the other end of the relay, so it is de-energized. The diode across the collapsing magnetic field (when the relay de-energizes) from damaging the transistor in the SALT.

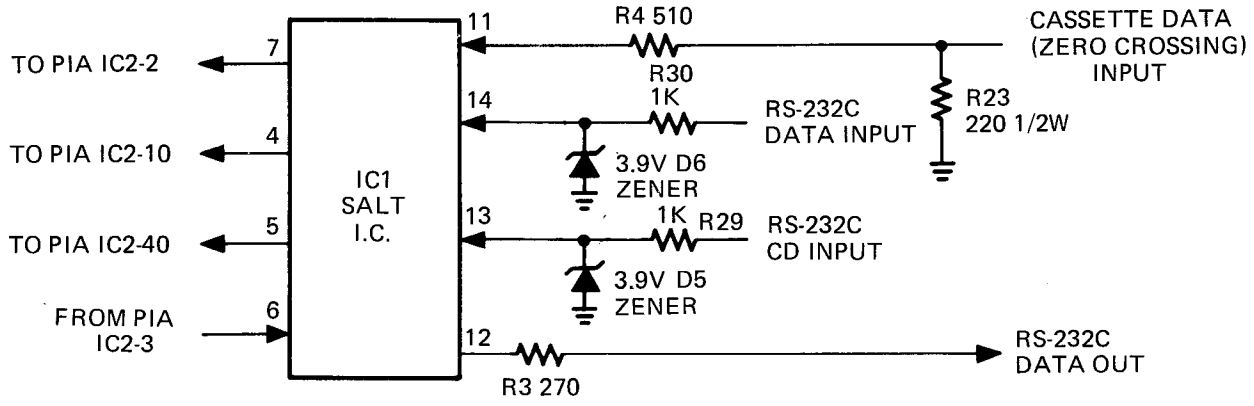


Figure 4-14. I/O Circuitry

4.11 Cassette Tape Format Information

The standard TRS-80 Color Computer 2 tape is composed of the following items:

1. A leader consisting of 128 bytes of 55H
2. A Namefile block
3. A blank section of tape equal to approximately 0.5 seconds in length to allow BASIC time to evaluate the Namefile
4. A second leader of 128 bytes of 55H
5. One or more Data blocks
6. An End of File block

The block format for Data blocks, Namefile blocks, or an End of File block is as follows:

1. One leader byte — 55 H
2. One sync byte — 3CH
3. One block type byte:
   01H = Data block
   FFH = End of File block
   00H = Namefile block
4. One block length byte — 00H to FFH
5. Data — 0 to 255 bytes
6. One checksum byte — the sum of all the data bytes plus block type and block length bytes
7. One trailer byte — 55H

The End of File block is a standard block with a length of 0.

The Namefile block is a standard block with a length of 15 bytes (0FH). The 15 bytes of data provide information to BASIC and are employed as described below:

1. Eight bytes for the program name
2. One file type byte:
   00H = BASIC Program
   01H = Data File
   02H = Machine Code Program
3. One ASCII flag byte — 00H = Binary, FFH = ASCII
4. One Gap flag byte — 01H = continuous, FFH = gaps
5. Two bytes for the start address of a machine language program
6. Two bytes for the load address of a machine language program

4.12 RS-232C Connector (JK3)

The RS-232C interface utilizes a 4-pin DIN connector. This interface allows the computer to have serial communications with printers, modems, other computers, or any device capable of interfacing with RS-232C signals. The four signals used by the interface are:

1. CD — a status line
2. RS-232C IN — serial data input
3. GROUND — zero voltage reference
4. RS-232C OUT — serial data out

The pinout for the DIN connector is shown in Figure 4-15, as viewed from the rear of the computer.

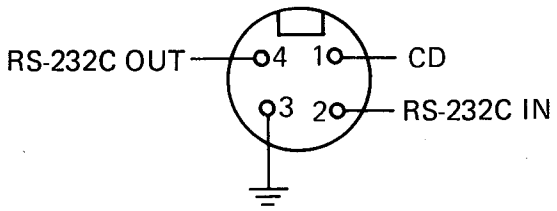


Figure 4-15. RS-232C Connector Pin-Out

The RS-232C interface hardware in the Color Computer 2 is capable of communication with any device which will operate with the minimum three-signal interface. It is also possible that devices which use a larger set of RS-232C signals may be used with the Color Computer 2. This would be accomplished by connecting unused device inputs to the correct high or low level.

In software, the only RS-232C device supported by the 8K BASIC ROM is a serial printer. For use with the printer, the pin assignment of the connector differs slightly from the above description:

1. No Connection
2. Connected to the BUSY output (or status line) of the printer
3. Ground
4. Connected to the Serial Data Input of the printer

If your printer does not provide a status line, then pin 2 must be connected to a positive voltage of +3 to +12 volts. This tells the computer that the printer is ready all of the time.

In order to operate, the software must make several assumptions about the printer. These assumptions are:

1. The printer operates at 600 Baud.
2. The printer width is 132 columns.
3. The printer generates a BUSY when it is not ready.
4. The printer will automatically return the carriage at the end of the line. It will also do a line feed at this time.
5. The data format is one start bit, eight data bits, two stop bits, and no parity.

Some printers will require that these assumptions be modified. This may be accomplished by changing RAM variables or by a special driver routine.

A list of all the printer variables is given in Table 1. Also, Table 1 lists some alternate values for these variables. The last comma field variable should be set equal to the width value minus the comma field width. The comma field width will normally stay at 16.

4.13 Cartridge Connector (CN1)

The 40-pin cartridge connector provides the possibility of expanding the TRS-80 Color Computer 2 in almost any manner. All of the important CPU bus signals are tied to this connector. A complete list and brief description of these signals is provided in Table 3.

The most common usage of the cartridge connector is with the ROM cartridge. For Cartridge detection, the Q clock is connected to the cartridge interrupt pin, which generates an interrupt anytime the cartridge is plugged in and forces the computer to jump to the program in ROM.

CAUTION

DO NOT PLUG A CARTRIDGE IN WITH POWER APPLIED TO THE COLOR COMPUTER 2 AS SERIOUS DAMAGE TO THE UNIT AND/OR THE CARTRIDGE MAY RESULT.

In addition to the expected data, address, and R/W lines, several control and special purpose signals are available on the Cartridge connector. They are as follows:

HALT* – This active low signal places the processor in a HALT state immediately following the execution of the current instruction. While in the HALTed state, the processor address and data lines are in the high impedance mode, making it possible for external devices to access RAM and ROM. The processor may be HALTed indefinitely without any loss of internal data.

NMI* – This is the non-maskable interrupt input to the CPU.

RESET* – This is the master system reset and power-up clear signal.

E, Q – These are the two clock signals for the MC6809E CPU.

CART* – This is an interrupt input into PIA IC2. It is used to detect the presence of a cartridge.

CTS* – This is the Cartridge Select Signal. It is valid when the processor reads any location from C000 Hex to FEFF Hex, as long as the SAM is in Map Type 0. Note that it is not active during a write to these locations.

SND – This signal is connected directly to the sound input of the DAC chip, and allows cartridge generated sound signals to be fed through the TV sound system. The signal should be AC coupled, and should not exceed 3.9 volts p-p.

SCS* – This is a second chip select signal from IC7. It is active for both reads from and writes to addresses FF40H through FF5FH, regardless of the map type.

SLENB* – This signal disables the internal device selection. This allows decoded but unused sections of memory to be used by the cartridge hardware.

4.14 Power Transformer

The Color Computer 2 power transformer accepts 120 VAC 60 Hz input and transforms it to 17.2 VAC center-tapped for use by the power supply. The current rating of the secondary of the transformer is 1.8 amps RMS maximum. The transformer should only be replaced with genuine Radio Shack replacement parts.

VARIABLE	HEXADECIMAL ADDRESS	DECIMAL ADDRESS	INITIAL VALUE HEXA-DECIMAL	DECIMAL
BAUD RATE MSB	0095	149	00	0
BAUD RATE LSB	0096	150	58	88
LINE DELAY MSB	0097	151	00	0
LINE DELAY LSB	0098	152	01	1
COMMA FIELD WIDTH	0099	153	10	16
LAST COMMA FIELD	009A	154	70	112
LINE PRINTER WIDTH	009B	155	84	132

Table 1. Line Printer Variables

BAUD RATE:	DECIMAL VALUE MSB	LSB	HEXADECIMAL VALUE MSB	LSB
120 BAUD	1	202	01	CA
300 BAUD	0	180	00	BE
600 BAUD	0	88	00	58
1200 BAUD	0	41	00	29
2400 BAUD	0	18	00	12
LINE DELAY:	**DECIMAL VLAUE MSB**	**LSB**	**HEXADECIMAL VALUE MSB**	**LSB**
.288 SECONDS	64	0	40	00
.576 SECONDS	128	0	80	00
1.15 SECONDS	255	255	FF	FF
WIDTH:	**DECIMAL VALUE**		**HEXADECIMAL VALUE**	
16 CHARACTERS/LINE	16		10	
32 CHARACTERS/LINE	32		20	
64 CHARACTERS/LINE	64		40	
255 CHARACTERS/LINE	255		FF	

Table 2. Alternate Line Printer Variable Values

PIN	SIGNAL NAME	DESCRIPTION
1	NC	
2	NC	
3	HALT*	Halt Input to the CPU
4	NMI*	Non-Maskable Interrupt to the CPU*
5	RESET*	Main Reset And Power-Up Clear Signal to the System
6	E	Main CPU Clock (0.89 MHz)
7	Q	Quadrative Clock Signal Which Leads E
8	CART*	Interrupt Input For Cartridge Detection
9	+5V	+5 Volts (300 MA)
10	D0	CPU Data Bit 0
11	D1	CPU Data Bit 1
12	D2	CPU Data Bit 2
13	D3	CPU Data Bit 3
14	D4	CPU Data Bit 4
15	D5	CPU Data Bit 5
16	D6	CPU Data Bit 6
17	D7	CPU Data Bit 7
18	R/W*	CPU Read–Write Signal
19	A0	CPU Address Bit 0
20	A1	CPU Address Bit 1
21	A2	CPU Address Bit 2
22	A3	CPU Address Bit 3
23	A4	CPU Address Bit 4
24	A5	CPU Address Bit 5
25	A6	CPU Address Bit 6
26	A7	CPU Address Bit 7
27	A8	CPU Address Bit 8
28	A9	CPU Address Bit 9
29	A10	CPU Address Bit 10
30	A11	CPU Address Bit 11
31	A12	CPU Address Bit 12
32	CTS*	Cartridge Select Signal
33	GND	Signal Ground
34	GND	Signal Ground
35	SND	Sound Input
36	SCS*	Spare Select Signal
37	A13	CPU Address Bit 13
38	A14	CPU Address Bit 14
39	A15	CPU Address Bit 15
40	SLENB*	Input to Disable Device Selection

Table 3. Cartridge Connector Signals

4.15 Joysticks

The optional joystick controllers are two identical assemblies which can plug into JK1 and JK2. Figure 4-16. shows a schematic of the Joystick Assembly. It consists simply of a push button switch for the fire button and the dual potentiometers connected by a mechanical assembly.

The mechanical assembly allows both potentiometers to be changed at the same time. This gives the effect of a two-dimensional control. The potentiometers are connected so that 5 volts is applied to one side of the variable resistor, and ground is connected to the other. This allows the center wiper to vary from 0 to 5 volts as the handle is moved. The push button switch merely provides a momentary ground contact for an input signal.

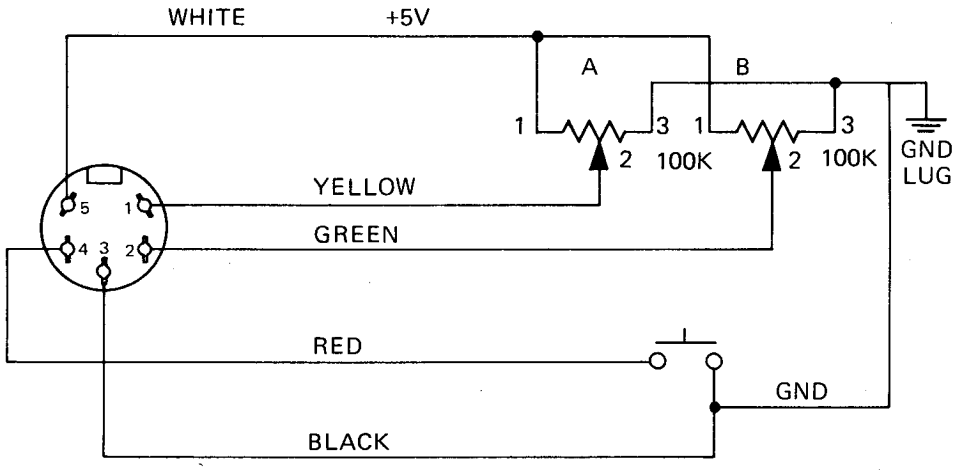


Figure 4-16. Joystick Schematic

4.16 TV Switch Box

The antenna switch box consists of a switch and a balun, with connectors provided for attachment to the computer, the TV antenna, and the home TV. The switch box is connected to the customer's TV through the 300 ohm twin-lead output. The TV antenna is attached directly to the switch box. The computer output is connected through a 75-ohm coax cable to the photo plug input on the switch box. Figure 4-17 shows a schematic of the antenna switch box.

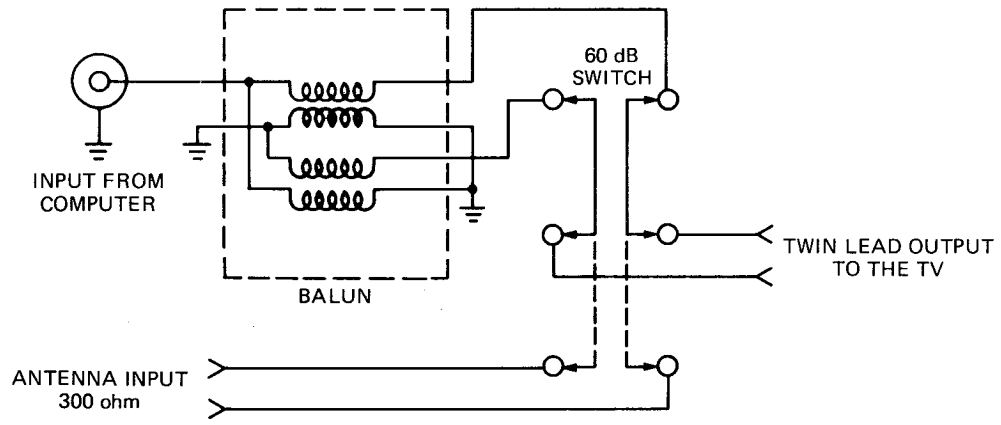


Figure 4-17. Antenna Switch Box Schematic

From the computer, the signal is connected to a balun in the switch box which matches the modulator's 75-ohm output impedance to a TV's 300-ohm antenna input impedance. This signal is then connected to the switch. The switch is specially designed to provide the 60 dB of isolation required between the computer and the TV antenna.

SECTION V

TROUBLESHOOTING

This section of the manual contains troubleshooting hints, diagnostic routines, and scope waveforms for the Color Computer 2. Scope settings are noted on the individual waveform diagrams.

5.1 Introduction

The Color Computer 2 should be serviced only by qualified technicians. Throughout this guide a basic knowledge of computers will be assumed, as will the ability to use a dual-trace oscilloscope. As is true when servicing any computer, it is important to distinguish between a hardware problem and a software problem. Stated another way, just because a particular program does not yield the results desired by the user, the hardware is not necessarily at fault. It is therefore recommended that the technician be thoroughly familiar with the operation of the Color Computer 2, as well as the Theory of Operation. Diagnostic aids are available from Radio Shack National Parts to assist the technician in the servicing of the Color Computer 2.

Standard troubleshooting techniques include the steps: identify, localize, and isolate. The first step, identify, consists largely of making sure that a problem exists. In this step it is wise to check the obvious. Doing so can save hours of troubleshooting time only to find out that a cable was bad, or that it was some other relatively minor problem. After identifying that a problem really does exist, localizing can usually be accomplished by merely observing the symptoms. Isolating a problem down to the defective component will often involve the use of test equipment, and sometimes, by part substitution.

Following is a list of virtually all of the problems that might be identified on the Color Computer 2:

Video
Keyboard
Processing problems
Cassette
RS-232C
Sound
Joystick
Cartridge problems

If a problem exists in more than one area, the first course of action should be to look for a common cause. Although it is possible to have two or more independent problems, it is more likely that a single failure can cause a multitude of symptoms. It is apparent, for example, that if the power supply is dead, that all of the above areas will have problems.

Once a problem has been identified in one of the above areas, it can be localized by observing the specific symptom. For example, if a Cassette problem exists, is it a Read problem, a Write problem, or a Motor Control problem? After the problem is localized, isolating it to a specific component is usually not very difficult. Included in this section is a flowchart for verifying proper operation of the power supply, oscilloscope pictures of various signals under proper operation, and a textual description of symptoms one might expect along with probable causes.

5.2 Video Problems

5.2.1 No Display

One of the first indications that the Color Computer 2 is working is the display on the T.V. If upon powerup the T.V. continues to display "snow", indicating that it is not receiving a signal from the computer, the first thing that should be done is to check the obvious. Is the proper channel selected on the T.V. and the computer? Is the coaxial cable connected from the computer to the T.V. switchbox? Is the switchbox connected to the VHF inputs of the T.V.? Is the switchbox in the "computer" position? On sets requiring it, is the 75 ohm VHF link connected to enable the 300 ohm inputs?

If the answer to each of the above questions is yes, then either the power supply or the modulator is dead. In this case, a quick check for the presence of +5 volts at the side of C32 should suffice to determine whether the power supply or the modulator is at fault. If the +5 volts is there, then the modulator should be replaced. If the voltage is incorrect or missing, proceed to the section on checking the power supply.

It is also possible to have no video, but instead of the screen remaining snowy, it is completely black or blank. In this case, the T.V. is at least receiving a signal from the computer, which indicates at least partial functioning of the power supply and modulator. However, there is still the possibility that one or the other of these components is at fault. There is also the possibility of some obvious "gotcha" – check that the proper channel is selected on both the T.V. and the computer, and that the brightness and contrast of the T.V. are set at an appropriate level. If these are O.K., then get out the oscilloscope and check for the Y signal at pin 28 of IC8. A normal Y signal is shown in Figure 5-6 (page 62). If the Y signal is present, then the modulator is the most likely suspect. If the Y signal is missing, then IC8 is probably at fault. Other possibilities include the power supply (do a complete check) and circuit board shorts or opens associated with IC8 and the modulator.

5.2.2 No Sync

If the image on the screen is not synchronized properly (it is rolling vertically or diagonally), then the most likely suspect is IC8 or the clock signal going to IC8. Of course, there is one obvious thing to check first – are the T.V. and the computer set to the same channel? If so, then scope out the 3.58 MHz clock signal going into pin 33 of IC8. This signal must be at the proper amplitude (TTL level) and the proper frequency (3.58 MHz). A normal clock signal is shown in Figure 5-5 (page 62). If the clock is O.K., then either the VDG (IC8) is bad, or the Y signal is loaded by a PCB short. It is also remotely possible that the modulator is bad.

If the clock signal is missing, or the wrong amplitude or frequency, proceed to the section on checking the clock.

5.2.3 "Garbage" on Screen

In many cases, a screenful of "garbage" (random characters) indicates a processing problem. To verify whether or not this is the case, try some simple commands that do not require screen output to prove they are working. For example, "SOUND 60, 20" or some similar sound command may be executed directly if one types carefully. "CLOAD" should also start the cassette and, if a short program is loaded, should stop at the end. If tests like these do not function, proceed to the section on Processing Problems.

If the above tests indicate that the processor is functioning normally, then the problem is likely caused by either bad RAMs, (IC14 – IC21), a bad latch (IC5), or a bad VDG (IC8). Substitution with known good RAMs should be used to isolate a RAM problem. For the other two possibilities, an oscilloscope should be used to check all signals for valid TTL levels. The latch should be clocked by the RAS* signal, which also appears at pin 4 of the RAM chips. If a bad logic level is found, then the chip producing the logic level is suspect. If no problem is found with the RAMs or the latch, the VDG should be checked by substitution (again, with a known good IC).

5.2.4 Clear Screen, No Sign on

When the Color Computer 2 is first powered up, it clears the screen and prints the appropriate BASIC sign on message. If the screen clears, but the signon fails to appear, there is most likely a processing problem. Particularly suspect would be an active FIRQ* without a cartridge present. Proceed to the section on processing problems.

5.2.5 No Color

Before attempting to fix a no-color problem in the computer, ensure that the T.V. is properly adjusted. The color level control must be set to an appropriate level and the tint control should be approximately centered. The fine tuning control, if present, must be properly adjusted, or no color will appear.

It is a good idea to try the computer on both channels (3 and 4) to determine if it is merely an adjustment problem. Also note that the computer will not generate color on a T.V. that depends on the Vertical Interval Reference (VIR) signal to be present. Some T.V.s that use the VIR signal to automatically adjust the color have a switch to defeat this feature; others do not. If the VIR option cannot be defeated, then color will not be produced on this T.V. as the computer does not generate the VIR signal.

If color is produced on one channel and not on another, it should be determined whether the computer or the T.V. is at fault. This may be done by trying several computers on the computer is determined to be at fault, the modulator should be replaced.

If the computer does not generate color on any T.V., several possibilities exist. The first thing to check is the presence of the 3.58 MHz clock into the modulator (pin A). A scope picture is shown in Figure 5-5 (page 62). If the clock is missing, or less than 100 mV p-p amplitude, the modulator will produce a black and white picture. Probable causes for this include R13 open or increased in value, C61 shorted or leaking, or the modulator itself. (If the clock source, which is the SAM chip, is not working the system will not even produce a black and white picture.)

After determining the clock signal to be O.K., the next thing that should be checked is the Chroma outputs of the VDG. The Ch B output (pin 9) should be some steady DC value greater than 0 volts and probably less than 2 volts—usually about 3/4 to 1 volt. The Phase A and Phase B (pins 11 and 10, respectively,) outputs should display waveforms shown in Figure 5-6 (page 62) thru 5-9 (page 63). Note that the relationship of the DC levels of Phase A and Phase B determines the color (photographs are given for screen colors of red, blue, and green). If any of the signals are missing or at improper levels, the VDG is suspect. If replacing the VDG does not cure the problem, then the signals are loaded by either PC shorts or again, possibly a bad modulator.

5.2.6 Wrong Colors

The procedure for troubleshooting wrong colors is basically the same as that for no color. Insure that the T.V. is properly adjusted, paying particular attention to the tint control, and then check the chroma signals coming out of the VDG. Note that an irregularity of the Phase A signal may be caused by the Artifacting circuit (IC4, Q2, and associated resistors, capacitors, and diodes).

5.2.7 No Artifacting Or Improper Artifacting

The artifacting circuit in the Color Computer 2 is responsible for generating burst in the high-resolution mode, so that this mode will be displayed in color. Failure of the artifacting circuit could result in one or more of the following symptoms: no color in the high-res mode, wrong color all the time, or left part of the screen shaded a different color from the rest of the screen. If no color is obtained in the high-res mode, then either the one-shot (IC4) is not operating, or the transistor (Q2) is not coupling this signal onto Phase A. (Consult the earlier theory of operation for a detailed description of how this circuit works.) Oscilloscope pictures of the artifacting circuit are shown in Figures 5-10 (page 64) thru 5-12 (page 64). One strange symptom is that of the left side of the screen being shaded a different color from the rest of the screen. This indicates that the one-shot is taking too long to time out, causing the level of Phase A to be shifted during the active portion of the video display. This may be caused by a defective IC4, by leakage or improper value of capacitor C26, or by increase in value of resistor R10.

5.3 Keyboard

5.3.1 No Keyboard Entry

No keyboard entry may be caused by a variety of factors. These include: broken flex cable which connects keyboard to main PCB, detective PIA IC7, a short to ground on any of the keyboard row inputs, or a defective keyboard. In particular, note that the capacitors on the joystick fire button leads (C15 and C18) might short and cause this problem.

5.3.2 Some Keys Inoperative

The most common cause of some keys not working when others do is an open somewhere – either on the keyboard itself, or in the connecting flex cable, or on the PC board. If an isolated key does not work, the problem is almost certainly on the keyboard itself. However, if a whole row or column of keys does not work (see the keyboard matrix on the schematic diagram), then any of the above is a possibility. Other possible causes are a defective PIA (IC7).

5.3.3 Wrong Character for Key Pressed

If a different character is displayed other than the one that should be displayed for a given key, the problem is most likely a short. Again, the short could be on the keyboard itself, in the connector, or on the PCB. All of the aforementioned possibilities should also be checked. One additional possibility is that of a defect in the processing section, particularly on the data bus.

5.4 Processing Problems

5.4.1 General

Processing problems are the most difficult to isolate. This is because there are so many possibilities. One of the most valuable tools for locating the cause of processing problems is the osilloscope. In many cases, it is sufficient to determine whether there is activity on a given line, and that the high and low levels are valid TTL levels. A half-level almost always indicates a problem, except in the case of tri-state outputs. Even a signal with tri-state outputs, when not tri-stated, should go to valid TTL levels. Observe the scope picture of the memory signals, Figure 5-16 (page 66). Note that although the data output line (bottom trace) goes to a half-level at times, that it also goes down to a valid logic 0 and up to a valid logic 1 at other times.

In addition to showing valid levels, a scope can tell you if the signal is happening at the appropriate time. Although it sometimes gets rather complicated to trigger off the appropriate combination of signals, this is possible if absolutely necessary. As an example, observe Figure 5-6 (page 62), the picture of Y and Phase B. Note that the small negative-going blip of the Phase B signal (bottom trace) happens at exactly the same time as the back porch of the horizontal sync pedestal of Y (top trace). This is evident because time is measured on the horizontal axis of the scope, and the blip is exactly under the back porch. (Recall from the previous discussion that this is where this blip needs to be to generate color burst). Another example that shows timing is Figure 5-4 (page 61), which shows the quadrature relationship of the E and Q signals.

5.4.2 Symptoms

There are several common symptoms of processor-type problems: the processor may "lock up" (appear to do nothing), it may "go wild" (randomly execute garbage instructions and appear to be doing something, but not what it is supposed to be doing), or it may function "almost" correctly, but not quite. Any of these symptoms may be caused by the same type of defect. Therefore, the following items, instead of being listed by symptom, comprise a processing check list for any type of processor-related problem.

5.4.2.1 E and Q

Check for the presence of E and Q. These signals should look like the ones in Figure 5-4 (page 61). If either clock is missing, the CPU will not operate. Also make sure that the clocks have good logic levels. The E clock is more demanding than the Q clock, and requires a high logic level of at least 4 volts. These clocks are produced by the SAM chip (IC22). E is sent to both PIAs (IC2 and IC7), the CPU (IC9), the NOR gate (IC10) and the edge connector. The Q clock goes only to the processor and the edge connector. Both clocks have small value capacitors on them to prevent harmonic radiation. If any of these components connected to these clock lines become shorted, it is likely to reduce the amplitude of the clock signal.

5.4.2.2 Interrupt/Halt/Reset

After power up, without a cartridge installed and without executing any program, the NMI* line (pin 2), the FIRQ* line (pin 4), the HALT* line (pin 40), and the RESET* line (pin 34) of the processor should all be high. In addition, the IRQ* line (pin 3) should have a 60 Hz pulse on it (it should have a short low-going pulse about every 16m Sec). If any of these lines are stuck low, you have found the problem. Replace the processor. If the condition still exists, find out what is pulling the line low, and repair it. If the IRQ line is low, the PIA IC7 could be bad, or a problem could exist in the address decoding section. (Once the PIA generates an interrupt, the processor must access the PIA to clear the interrupt.)

5.4.2.3 Address/Data Lines

It is rather difficult to define exact patterns of address and data lines on the CPU as these are dependent upon which address is being accessed, and the data to be read or written. All address and data lines should be capable of activity, however, and the output levels should be valid TTL. Figure 5-13 (page 65) and 5-14 (page 65) show typical address and data patterns. Note that some of the address lines may not show activity when the processor is in a loop. However, by depressing the RESET button while scoping the address lines, at least momentary activity should be displayed. Another clue is that typically (although certainly not always) the address lines should act more or less like a frequency divider – that is, the frequency of activity on A1 should be half the frequency of activity of A0 and twice the frequency of A2, and so on. This is because the processor accesses intructions sequentially until the program counter is altered.

If any of the address or data lines seem incapable of generating either a valid logic 1 or valid logic 0, a fault is indicated. If the fault persists after replacing the CPU (IC9), then a device which is on the appropriate bus is probably shorted, or there is a PCB short.

5.4.2.4 Address Decoding Section

If the CPU is functioning normally, outputting all of the correct addresses, but the appropriate device (ROM, RAM, PIA, etc.) is not selected, a processing problem will be evident. During the "idle" mode (after power up but before accepting keyboard entry), the CPU should be alternately accessing the ROM (IC12 to obtain instructions) and the Keyboard PIA (IC7 looking for keyboard entry.) The ROM chip enable line (IC12, pin 20) should show activity, as should the PIA chip enable (IC7, pin 23). If either of these signals is absent, likely suspects are the SAM chip (IC22), the 3-to-8 decoder (IC11) or the NOR gate (IC10). The SAM should be checked by substitution, or by observing the S0 through S2 lines (pins 25, 26 and 27) on the oscilloscope. The decoder (IC11) can be easily checked with an oscilloscope for proper inputs and outputs, as can IC12. A final remote possibility is that the ROM (IC12) and the PIA (IC7) are loading the output signals of the decoder (IC11), or that PCB faults exist.

5.4.2.5 Memory Problems

If the ROM is being enabled frequently and all other CPU signals are good, but the screen never clears or the screen does clear but the signon does not appear, then either a ROM or RAM problem is indicated. These should be checked by substitution with known good devices. ROM and RAM faults could also be responsible for other processing type problems, such as intermittent lock-up, random (garbage) execution, the display of error messages when no error was committed, and incorrect results of computations. The last two cases require careful analysis of the attempted program or command before assuming a ROM or RAM problem. Some typical RAM waveforms (RAS*, CAS*, DATA IN and DATA OUT) are shown in Figure 5-15 (page 66) and 5-16 (page 66).

5.5 Cassette Problems

5.5.1 Motor Control Problems

Of all possible problems in the Color Computer 2, lack of motor control is probably the easiest to isolate. Of course, the obvious should not be overlooked, which includes bad cable or bad cassette recorder. Actuation of the relay can be tested by listening for the relay click while depressing the Reset button. If the click is heard, but continuity does not appear at pins 1 and 3 (the two outside pins) of the cassette connector, JK4, then either the relay is bad or the PCB or connector is open. If the click is not heard, then possible bad components are IC2, IC1, and the relay itself (open coil), as well as PCB faults. The following simple program will allow checking of these components:

```
10  POKE 65313,60
20  GOSUB 100
30  POKE 65312,52
40  GOSUB 100
50  GOTO 10
100 FOR A=1 TO 100:NEXT A:RETURN
```

After this program is keyed in and run, Scope IC2 pin 39 for a squarewave of approximately 20 Hz. If it is not present, then change IC2. If it is present, then scope IC1 pin 9 for the same squarewave. If it is not there, then change IC1. If it is there, then change the relay. If replacing the suspect component does not correct the problem, then a PCB fault is indicated.

5.5.2 Write Problems

Cassette write problems are also very simple to isolate and repair. Again, don't forget to verify the obvious, such as the cassette recorder and cable. If you are convinced that a cassette write problem exists, key in and execute the following program:

```
10  SOUND 200,255:GOTO 10
```

Now look for the waveforms as shown in Figure 5-17 (page 67). If the top waveform is there, but the bottom one isn't, look for it directly at the chip (IC3 pin 17). If it is at the chip, but not at the connector, PCB fault or connector fault is indicated. If it is not present at the chip, insure that pin 17 is not shorted to ground. If not, replace IC3 and re-run the program. If the waveform is still not present, the replace PIA IC7 and repeat the test. Remember that the cassette output amplitude should be somewhere between 1 and 2 volts p-p.

5.5.3 Read Problems

Isolating a cassette read problem is not much more difficult. However, to do so requires an input signal of some kind. A sufficient signal can be the cassette output signal coupled back to the cassette input through a 10 microfarad capacitor. Run the same program as above and look for the waveforms in Figure 5-15 (page 66). If the bottom waveform is not present (the input to the SALT chip, IC1), then check input components C23, R23, and R4, as well as the PCB and connector. If the input waveform is present, but not the output waveform, then replace the SALT chip (IC1). If the output is still not present, then look for PCB faults or PIA IC2 to be loading the output waveform. Remember, the input must go both above and below ground, and should be at least 100 mV p-p. Also, the output should be valid TTL levels.

5.6 RS-232C Problems

5.6.1 Output Missing or Incorrect

RS-232C problems are just about as easy as cassette problems. The output may be checked by entering in the following short program, running it, and scoping the output at JK3 pin 4:

```
10  POKE 65312,2
20  POKE 65312,0
30  GOTO 10
```

A square wave of approximately 40 Hz should appear. The square wave should go at least 3 volts negative and at least 3 volts positive. If the output is not there, look for it directly at the chip (IC1 pin 12). If it is still not there, change IC1 and try again. If the output is still not there, change PIA IC2 or look for PCB faults. If the output is at IC1 pin 12 but not at the edge connector, check current-limiting resistor R3, or look for PCB faults. It is possible to have a positive-going output, but not the negative going portion, as this is the only circuit in the computer that utilizes the negative portion of the power supply. Check for negative voltage (—7.5 or better) at IC1 pin 15. If it is not there, proceed to the Power Supply flowchart. If it is there, but there is no negative portion to the RS-232C output waveshape, then IC1 is most likely at fault.

5.6.2 Input Problems

RS-232C input problems can be checked in a static condition. Ground pin 1 of JK3 and insure that IC1 pin 5 goes high. Then connect pin 1 of JK3 to +5 volts and insure that IC1 pin 5 goes low. Repeat the test with JK3 pin 2 and IC1 pin 4. If any of the conditions are not met, then replace IC1. If problems still exist, then change PIA IC2 or check for PCB faults.

5.7 Sound Problems

Almost any sound problem in the Color Computer 2 can be traced to IC3. Other possibilities include PIA IC2 and the modulator. As a quick check, key in the following program and look for the waveform shown in Figure 5-17 (page 67) at the modulator, sound IN:

```
10 SOUND 200,255: GOTO 10
```

If the waveform is present but no sound is heard, replace the modulator (did you check to see if the volume control on the T.V. was turned up?). If the waveform is not present, then change IC3 or IC2 as necessary. If the problem still exists, check for PCB faults.

5.8 Joystick Problems

As with sound problems, joystick problems are almost always associated with IC3. Additional possibilities include IC2 for joystick pots, and IC7 for fire button problems. Of course, PCB and connector faults could also be a problem. To test the joysticks, connect two KNOWN GOOD joysticks and key in and execute the following program:

```
5 CLS
10 A = JOYSTK (0)
20 B = JOYSTK (1)
30 C = JOYSTK (2)
40 D = JOYSTK (3)
50 E = (PEEK (65280) AND1)
60 F = (PEEK (65280) AND2)/2
70 PRINT @ 0, A, B, C, D, F, E
80 GOTO 10
```

The top two numbers on the screen represent the right joystick. By rotating the joystick, you should be able to get each number to change from 0 to 63 and include all numbers in between. The next two numbers represent the left joystick, which should be tested in the same manner. The bottom two numbers represent the two fire buttons, and will be 1 when the fire button is not depressed and 0 when the fire button is depressed. (The left number is the left fire button and the right number is the right fire button.)

If any of the above testing does not yield the desired results, replace the components discussed above.

5.9 Cartridge Problems

In checking any kind of symptom dealing with an external cartridge, the obvious first step is to be sure that you are using a known good cartridge. If a known good cartridge causes the computer to lock up or execute random garbage, the most likely cause would be open address or data lines to the edge connector. To check this, use a dual trace oscilloscope, and check each address and data line, with one probe at the processor and the other at the connector. You should, of course, see identical signals. One other possibility that could cause this symptom would be a "dual addressing" type of problem, which would allow more than one device at a time to be activated. This would most likely be caused by the address decoding circuit consisting of SAM (IC22) and IC10 and IC11.

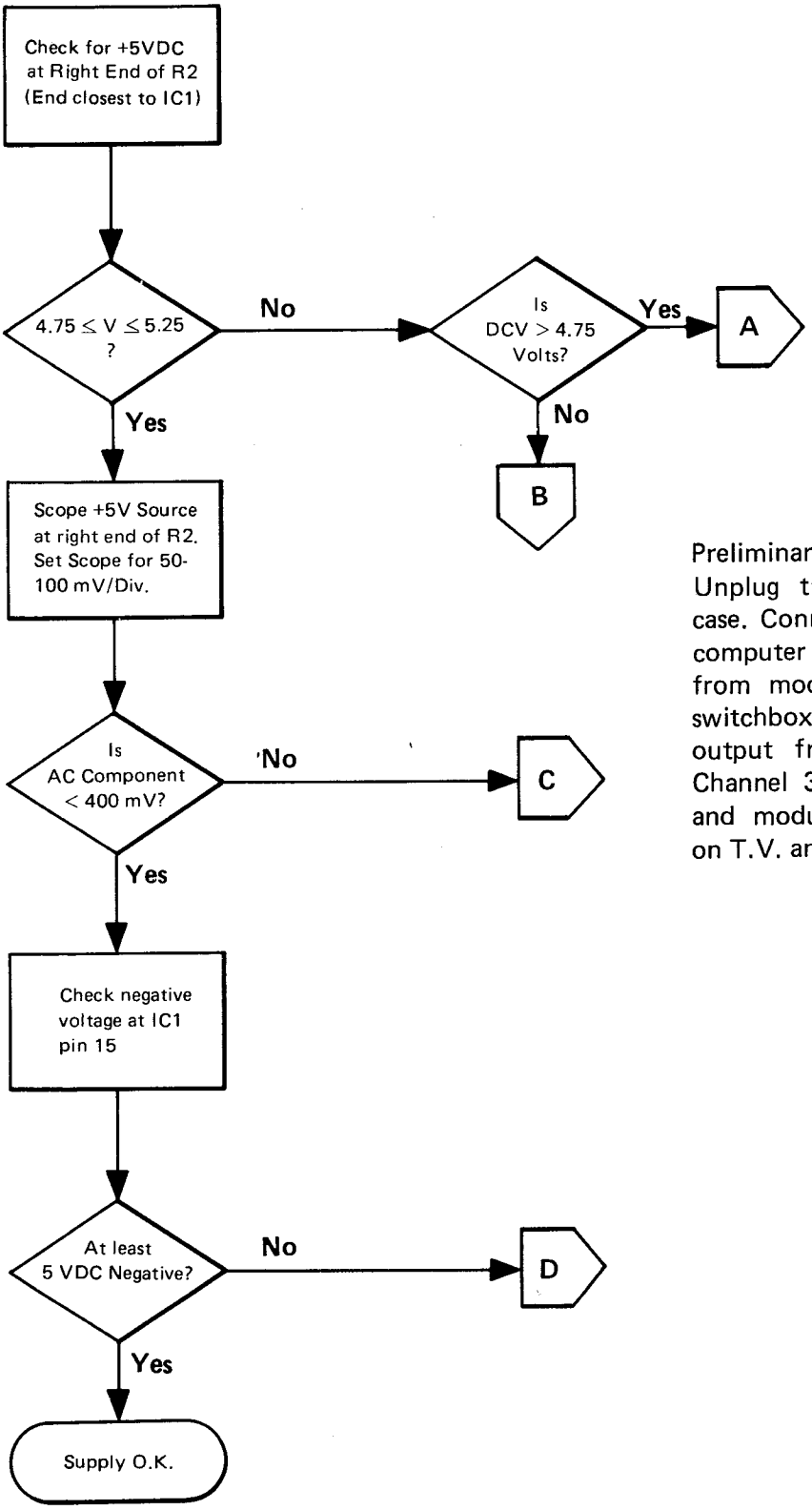
If the cartridge does not auto start, the lines Q and CART* should be checked for opens to the connector.

5.10 Power Supply

The Color Computer 2 power supply must function properly for the unit to work. Following is a flowchart for complete testing of the power supply. The power supply should be checked without any I/O devices or cartridges attached, as a defective external load could confuse the findings. In addition to tight (±5%) regulation of the DC voltage, the power supply should be relatively free of AC ripple or high frequency noise. Refer to Figure 5-3 (page 61) as well as the flowchart for information on AC content. If the power supply is "almost" functioning correctly, but not quite, the symptoms could be quite bizarre, as well as highly intermittent.

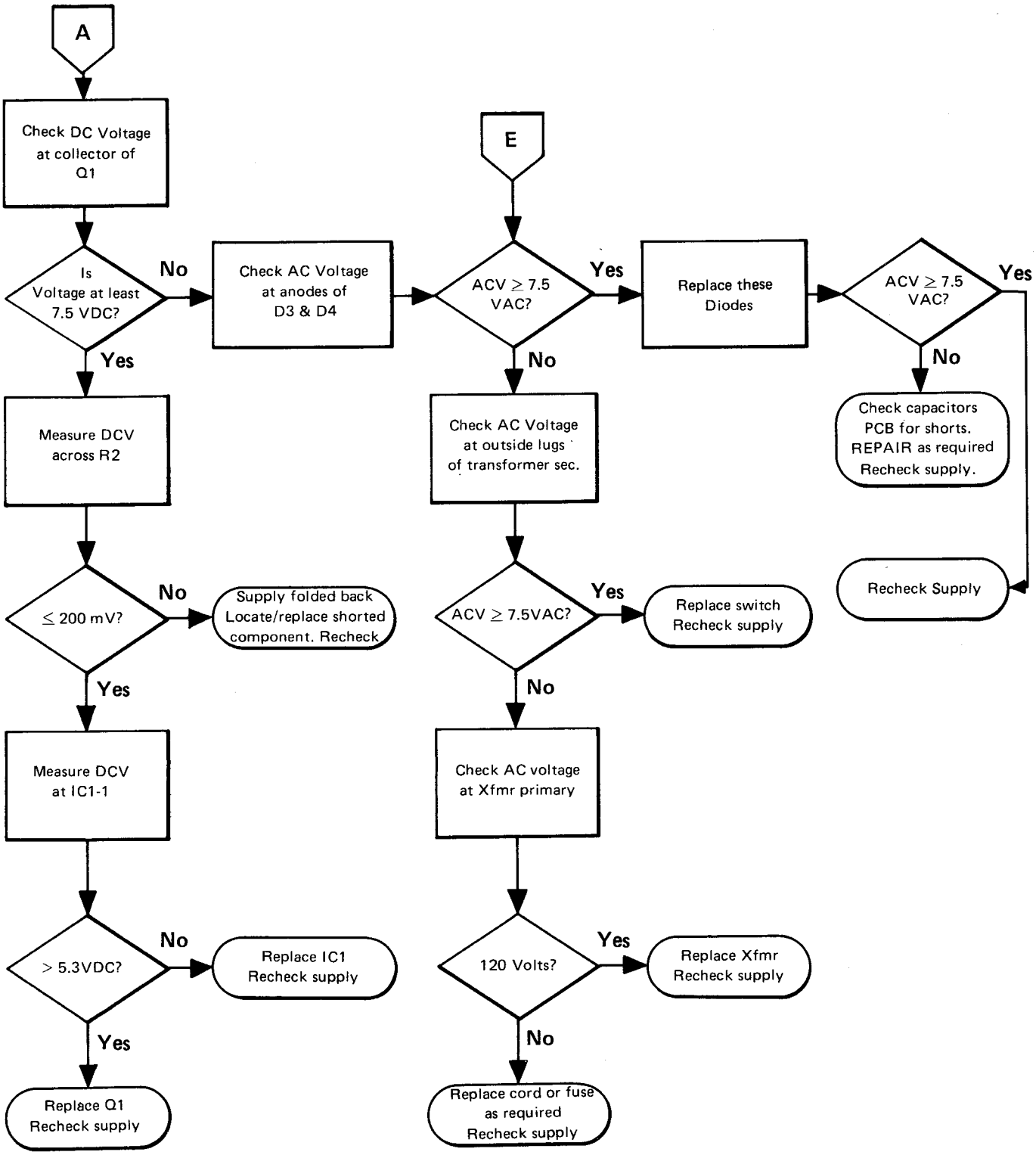
Of particular interest is the case where the power supply is acting in a half-wave configuration rather than a full-wave configuration (compare Figures 5-1 (page 60) and 5-2 (page 60)). This causes twice the AC ripple to be on the supply, and reduces the amount of current that can be drawn from the supply. Therefore, the computer might work "normally" without a plug in cartridge, but not function at all with a heavier load. A half-wave supply would also cause the pass transistor to get hotter than normal, and could cause premature failure.

Power Supply Check



Preliminary:
Unplug the computer. Remove the top case. Connect scope probe ground lead to computer ground. Connect coaxial cable from modulator output to TV/computer switchbox. Connect the 75 ohm twin lead output from switchbox to T.V. Select Channel 3 or 4 as desired on both T.V. and modulator. Plug in computer. Turn on T.V. and computer.

Power Supply Check (continued)



Power Supply Check (continued)

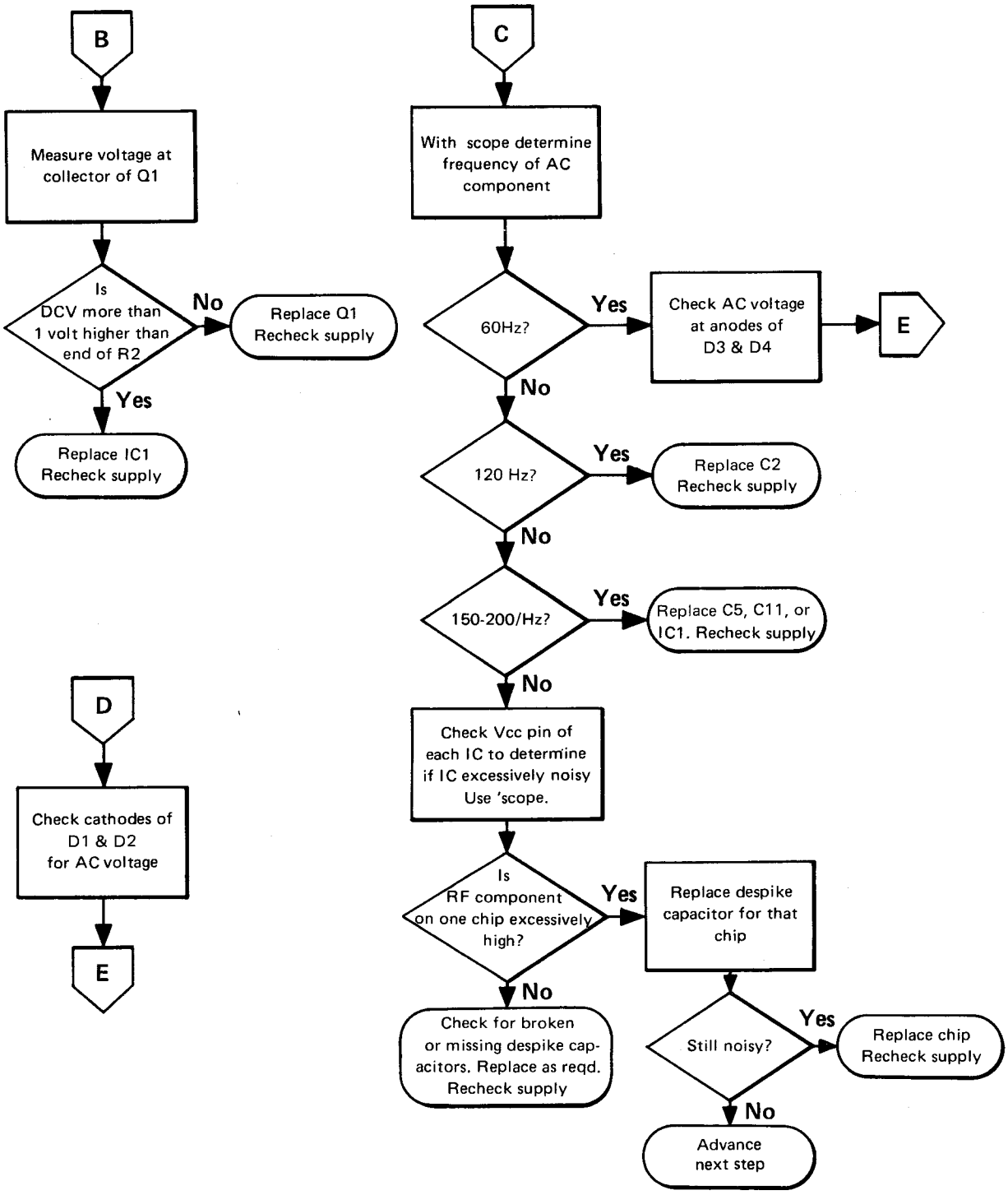
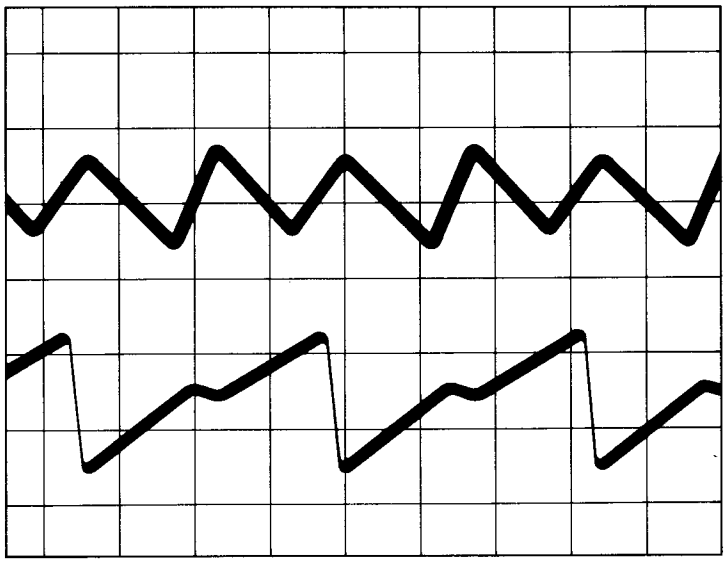


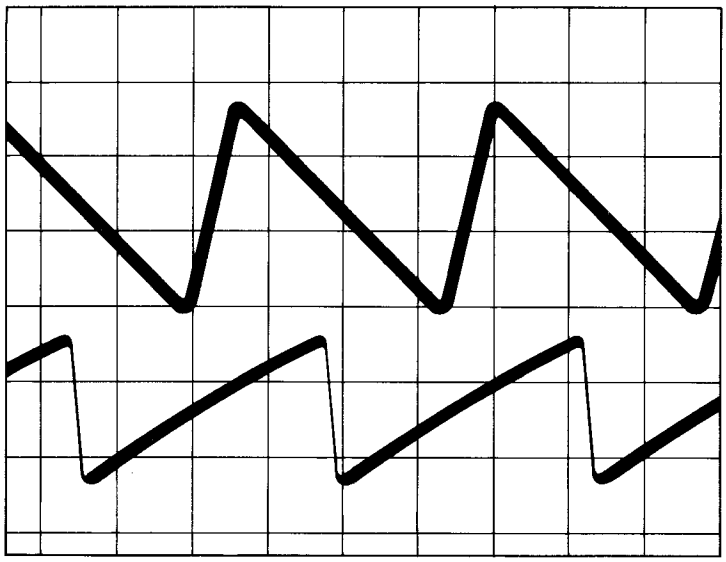
Figure 5-1



Normal Power Supply
(120 Hz ripple)

CH. A — Cathodes of D3, 4
.5 V/division
AC coupled
CH. B — Anodes of D1, 2
.2 V/division
AC coupled
Horizontal — 5 msec/div.
Trigger — Internal, CH. A
Slope positive

Figure 5-2



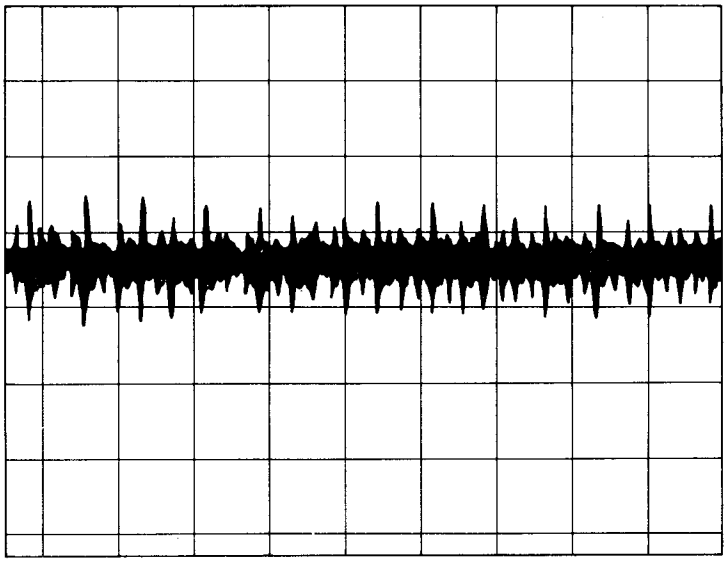
Defective Power Supply
(60 Hz ripple)

All settings same as above. One transformer lead pulled loose to simulate open diode.

Note that ripple frequency has changed from 120 Hz to 60 Hz and that ripple has increased from approximately 1V p-p to 2V p-p.

Although this computer might appear to function, the regular transistor gets excessively hot and erratic operation would likely follow.

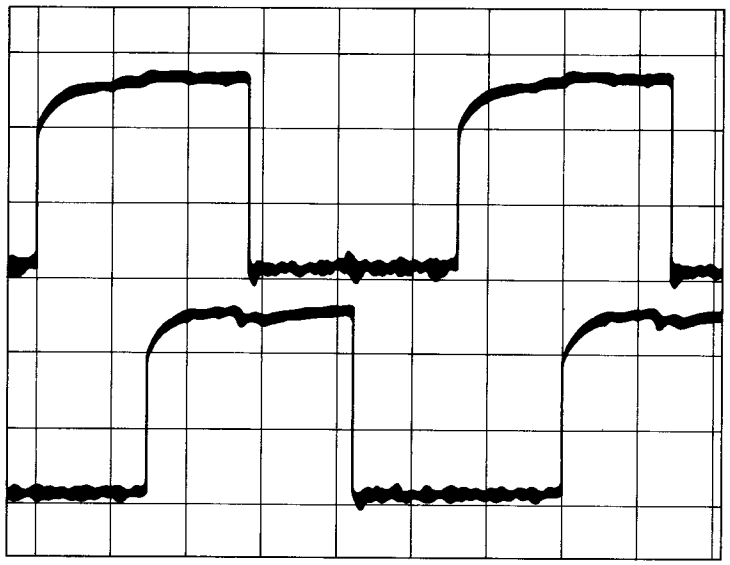
Figure 5-3



CH. A — +5 V Source (e.g. IC21 — 8)
100 mV/division
AC coupled
Horizontal — 0.5 μsec/division
Trigger — Internal, CH. A

High Frequency Component of +5 V Source

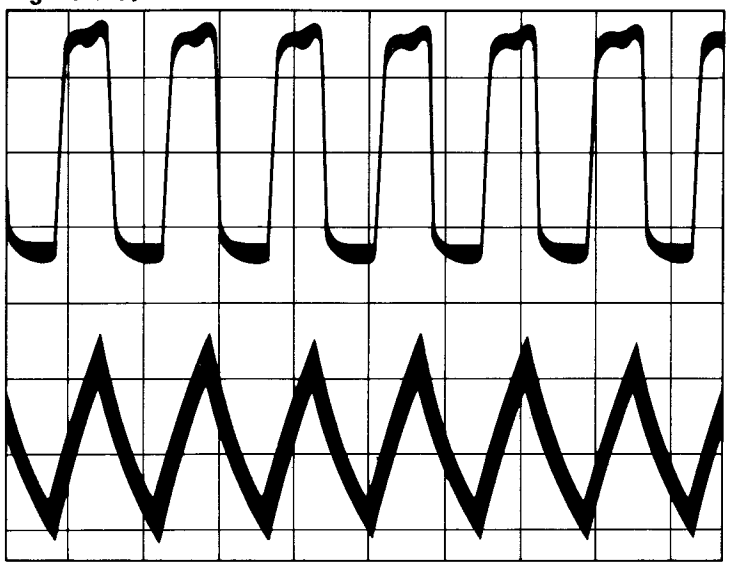
Figure 5-4



CH. A — Q clock (Top R24)
2 V/division
DC coupled
CH. B — E clock (Top R26)
2 V/Division
DC coupled
Horizontal — .2 μsec/Div
Trigger — Internal, CH. A
Slope positive

E & Q Clocks

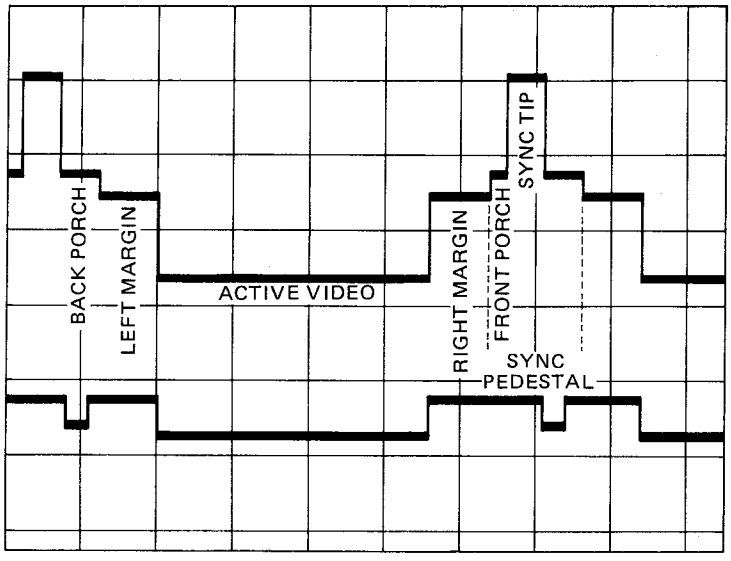
Figure 5-5.



VDG Clock (top) and Modulator Clock (bottom)

CH. A — IC8 pin 33
1 V/division
DC coupled
CH. B — Modulator, Top R13
50 mV/division
AC coupled
Horizontal — .2 μsec/division
Trigger — Internal, CH. A
Slope Negative

Figure 5-6



Y and ϕB

CH. A — Y (IC8 pin 28)
.2 V/division
AC coupled
CH. B — ϕB (IC8 pin 10)
1 V/division
DC coupled
Horizontal — 10 μsec/division
Trigger — Internal CH. A
Slope positive

Note: The dip in the Phase B signal that occurs during back porch time. This unbalances the balanced Modulator inside the 1372 chip (inside the Modulator), causing it to generate the 3.58 MHz Burst Signal for the T.V.
This picture was taken with a standard green screen.

Figure 5-7

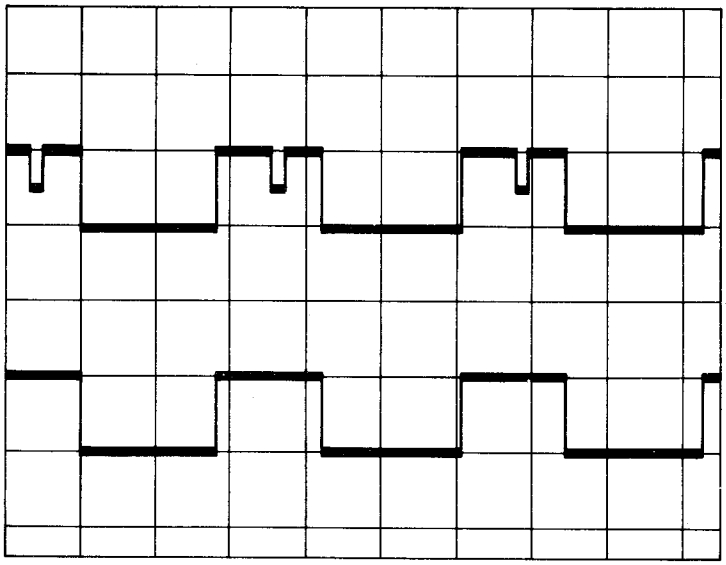


Figure 5-8

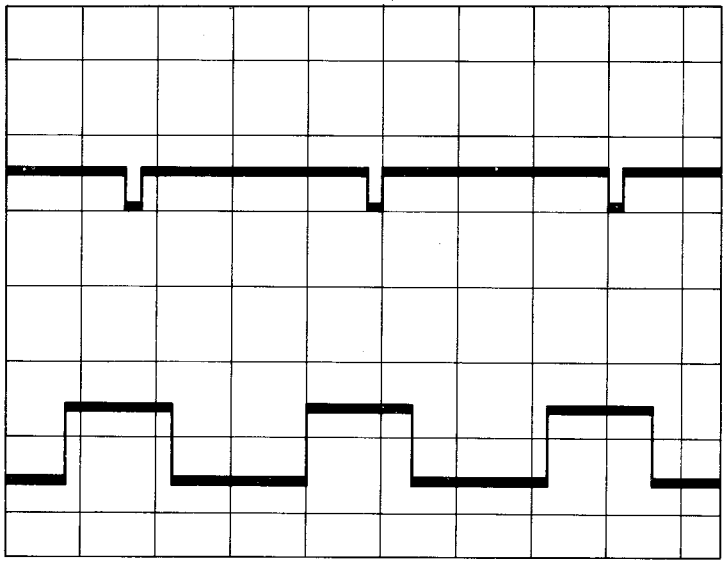
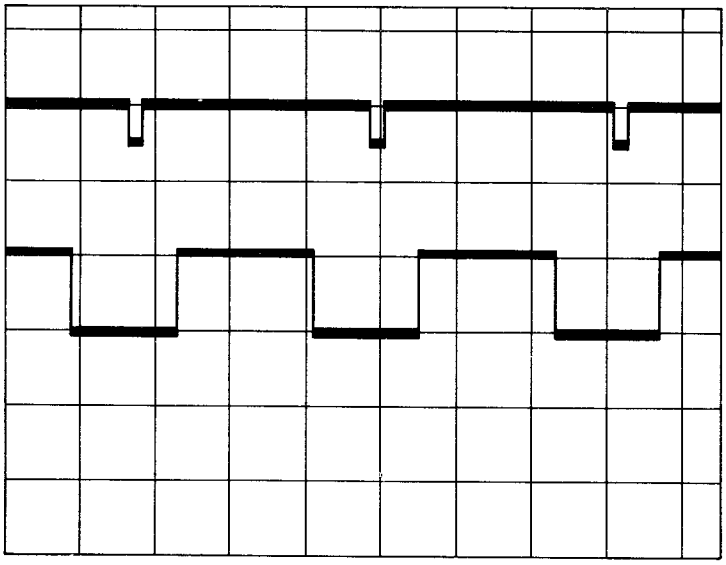


Figure 5-9



ϕB and ϕA Phase

Relationships for Different Colored Screens

Top — Green screen
10 CLS
20 GOTO 20

Middle — Cyan screen
10 CLS 6
20 GOTO 20

Bottom — Red screen
10 CLS 4
20 GOTO 20

Note: The different D.C. levels present during active video time for each color. Also note "burst dip" in ϕB, regardless of color.

For All 3 Pictures:

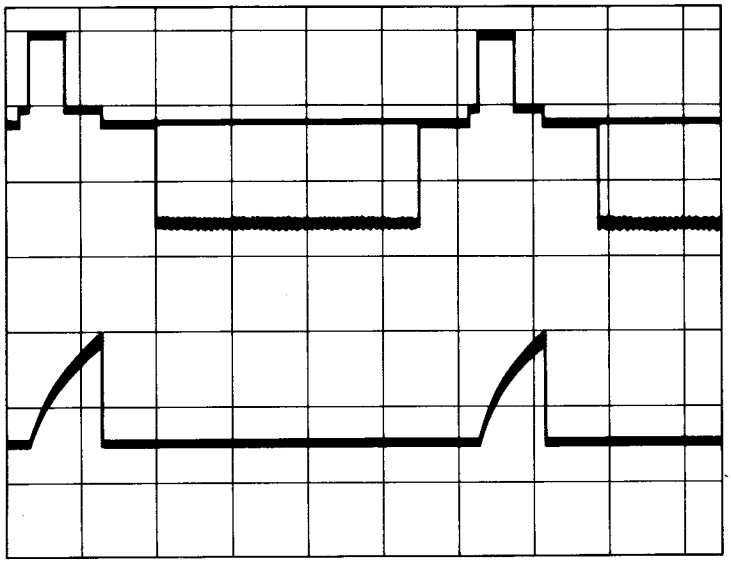
CH. A — ϕB, IC8 – 10
.5 V/division
DC coupled

CH. B — ϕA, IC8 – 11
0.5 V/division
DC coupled

Horizontal — 20 μsec/division

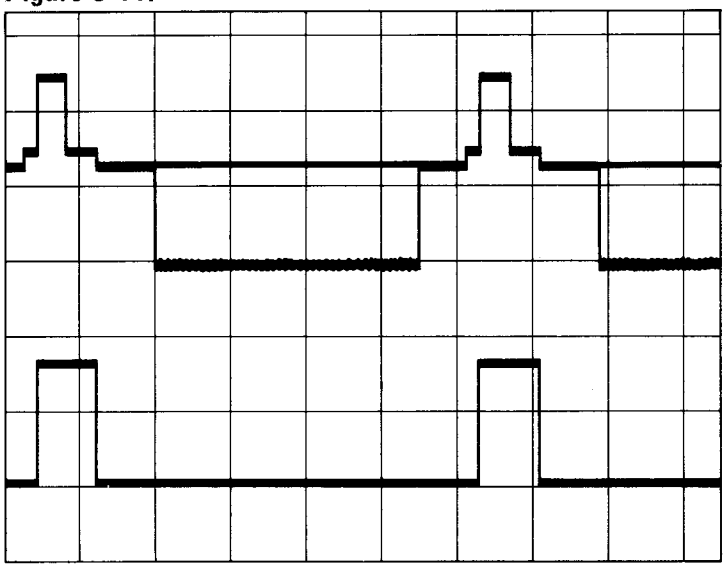
Trigger — Internal, CH. A
Slope positive

Figure 5-10.



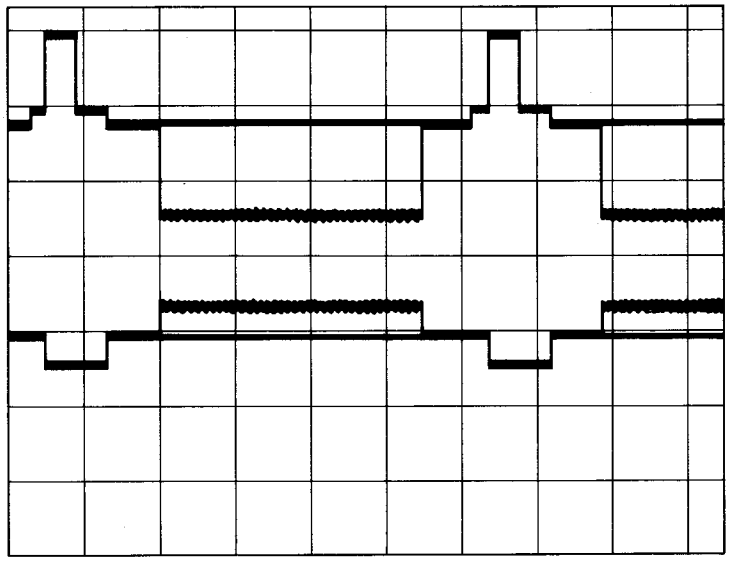
Artifacting Signals

Figure 5-11.



Artifacting Signals

Figure 5-12.



Artifacting Signals

Artifacting Signals

To check, the computer must be in the High-Res mode. To accomplish this, run the following program (pay no attention to garbage on the screen):

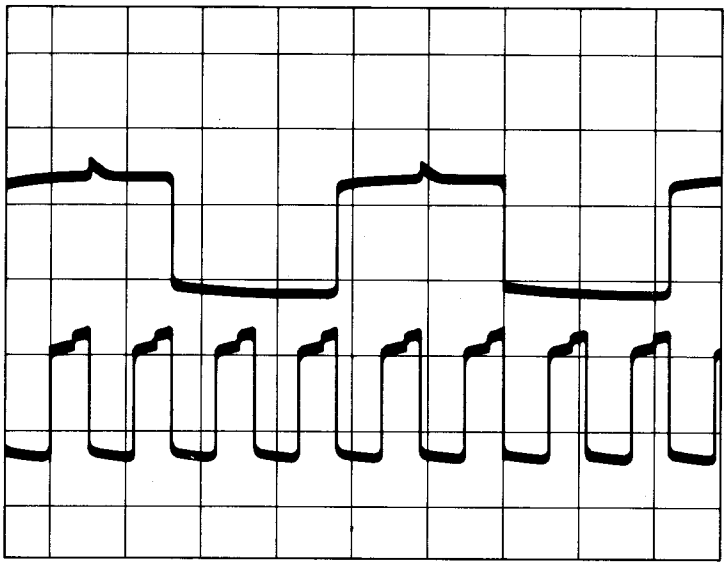
```
10          POKE 65314, 24
20          GOTO 20
```

CH. A — Y (IC8 pin 28)
.2 V/division
AC coupled
CH. B — IC4 pin 6
2 V/division
DC coupled
Horizontal — 10 μsec/division
Trigger — Internal, CH. A
Slope positive

CH. A — Y (IC8 pin 28)
.2 V/division
AC coupled
CH. B — IC4 pin 3
2 V/division
DC coupled
Horizontal — 10 μsec/division
Trigger — Internal, CH. A
Slope positive

CH. A — Y (IC8 pin 28)
.2 V/division
AC coupled
CH. B — Phase A (IC8 — 11)
1 V/division
DC coupled
Horizontal — 10 μsec/division
Trigger — Internal, CH. A
Slope positive

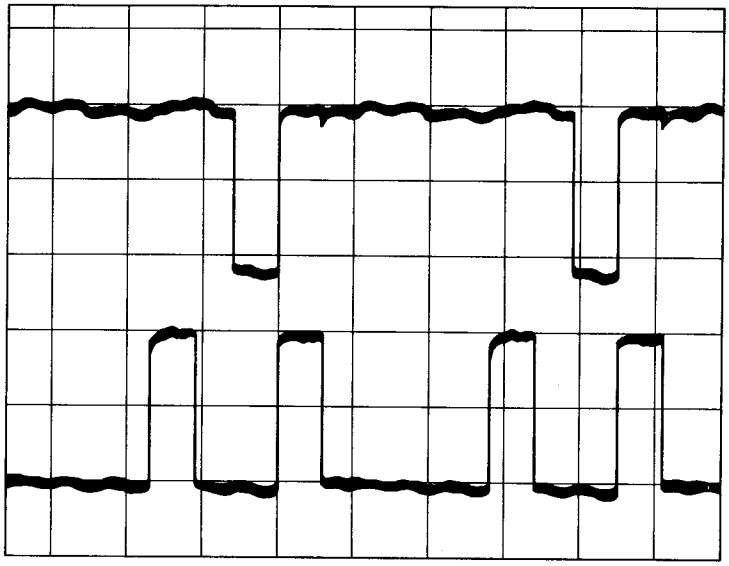
Figure 5-13



Address Lines (Typical)

CH. A — A9 (IC9, pin 17)
2 V/division
DC coupled
CH. B — A7 (IC9, pin 15)
2 V/division
DC coupled
Horizontal — 2 μsec/div.
Trigger — Internal, CH. A
Slope positive

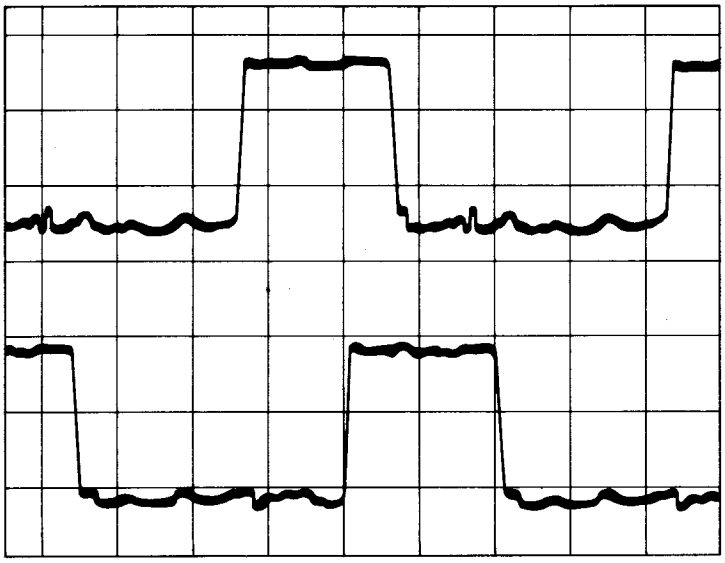
Figure 5-14



Data Lines (Typical)

CH. A — D2 (IC9, pin 29)
2 V/division
DC coupled
CH. B — D3 (IC9, pin 28)
2 V/division
DC coupled
Horizontal — 2 μsec/div.
Trigger — Internal, CH. A
Slope positive

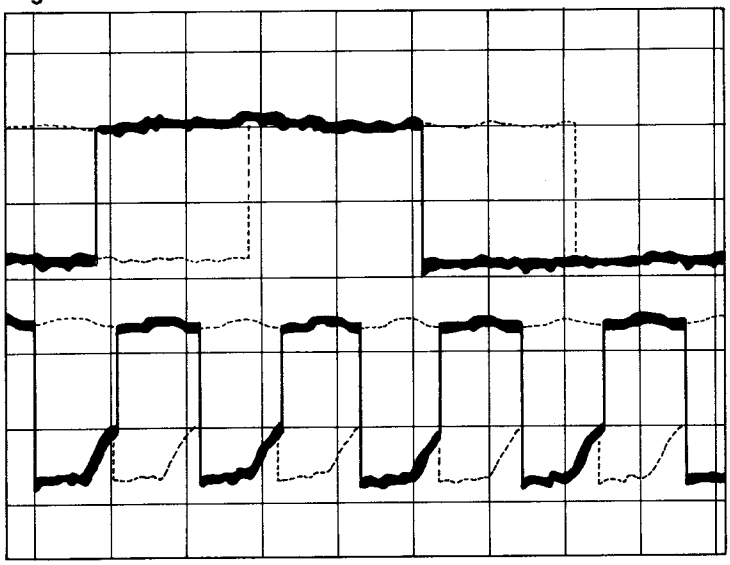
Figure 5-15



RAS* and CAS*

CH. A — RAS* (IC19-4)
2 V/division
DC coupled
CH. B — CAS* (IC19 – 15)
2 V/division
DC coupled
Horizontal — .1 μsec/div.
Trigger — Internal, CH. A
Slope nègative

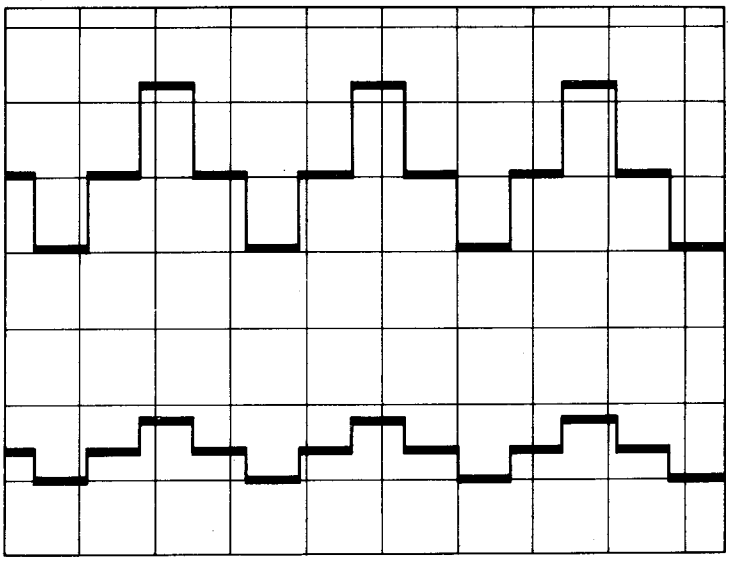
Figure 5-16



Data In and Data Out
Memory Signals

CH. A — Data in (IC19-2)
2 V/division
DC coupled
CH. B — Data out (IC19 – 14)
2 V/division
DC coupled
Horizontal — .5 μsec/div.
Trigger — Internal CH. A

Figure 5-17

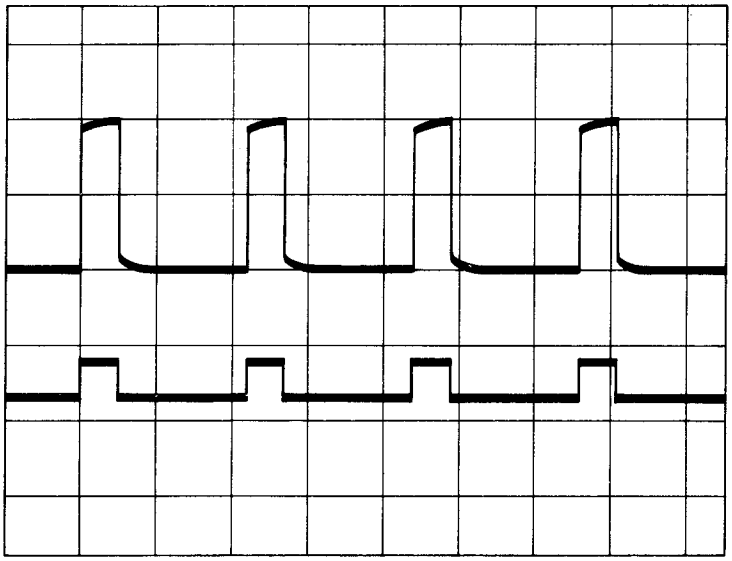


Sound & Cassette Output

CH. A — Sound out (IC2 pin 1)
2 V/division
DC coupled
CH. B — Cassette out (JK4 – 5)
2 V/division
DC coupled
Horizontal — .5 msec/div.
Trigger — Internal, CH. A
Slope positive

```
10 sound 200, 255: GOTO 10
```

Figure 5-18



Cassette Zero Crossing Detector

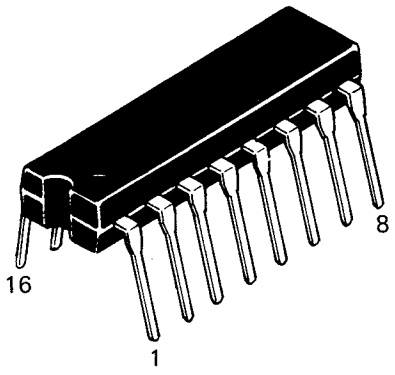
CH. A — Cassette Zero Crossing
Detector (IC1 pin 7)
DC coupled
CH. B — Cassette input (JK4 – 4)
.5 V/division
DC coupled
Horizontal — .5 msec/div.
Trigger — Internal, CH. B
Slope positive

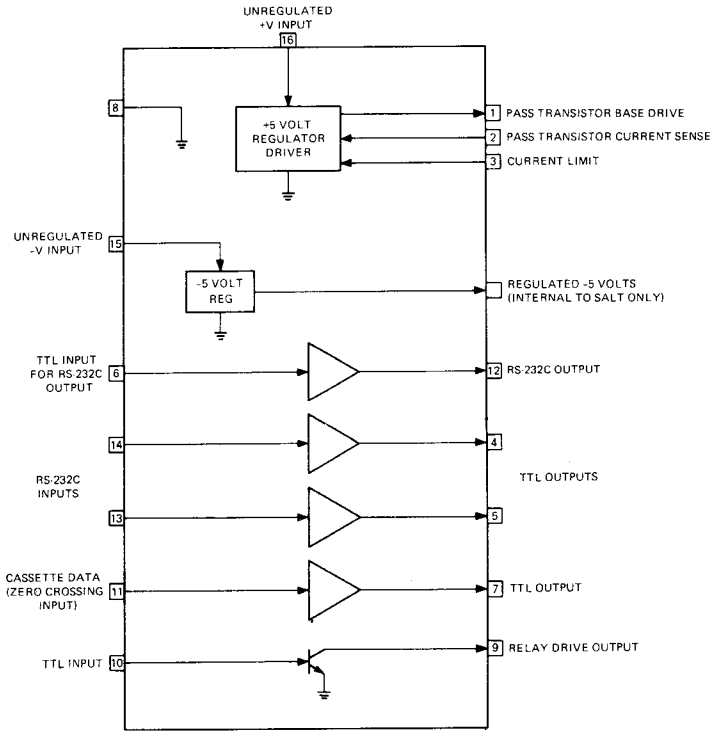
Note: The cassette output signal (JK4 – 5) is coupled back to the cassette input signal (JK4 – 4) through a 10 μF. The same program as above must be executed.

SECTION VI

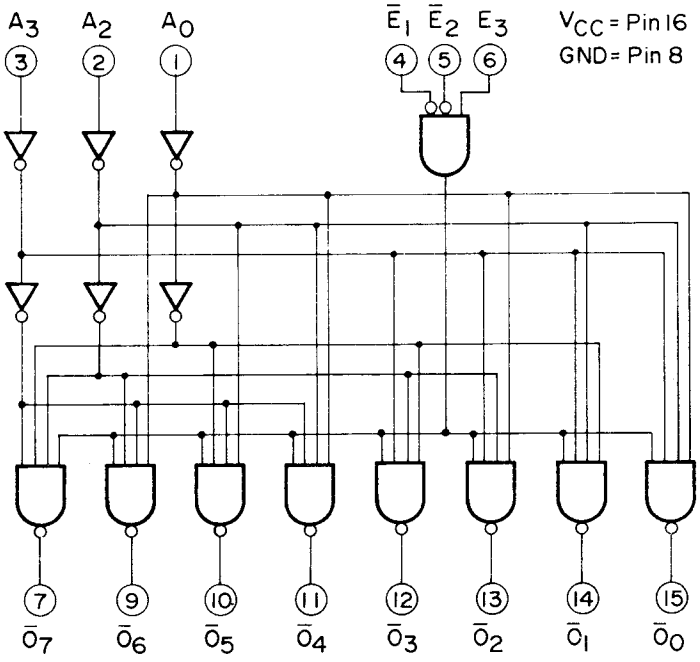
IC INTERNAL CONNECTIONS

IC1 SALT SC77527P

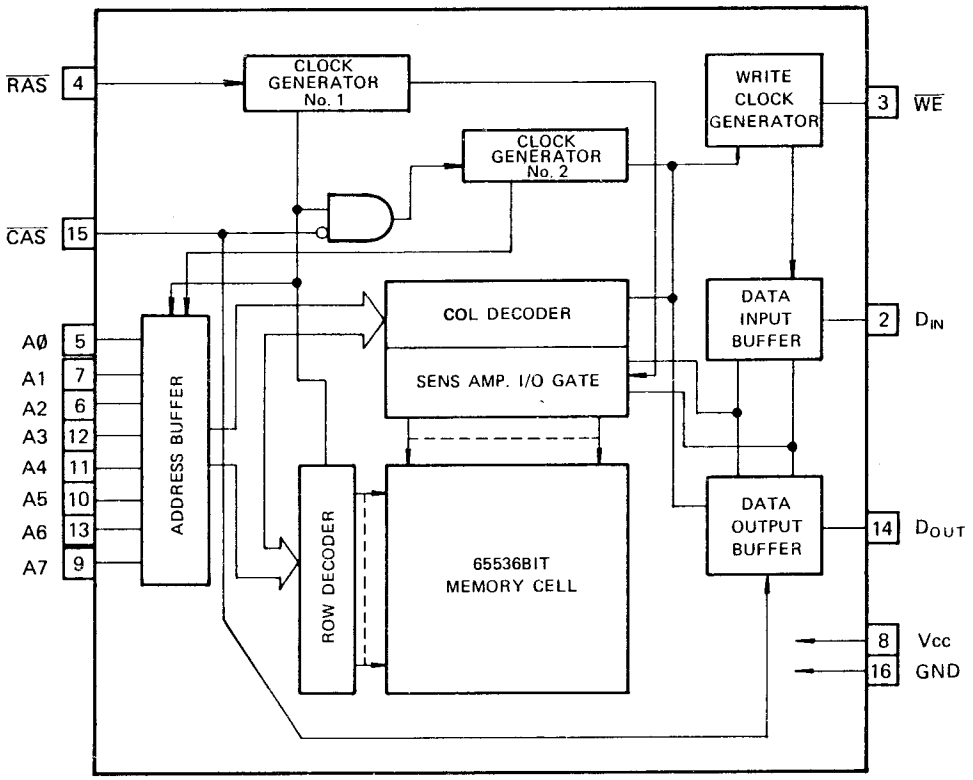




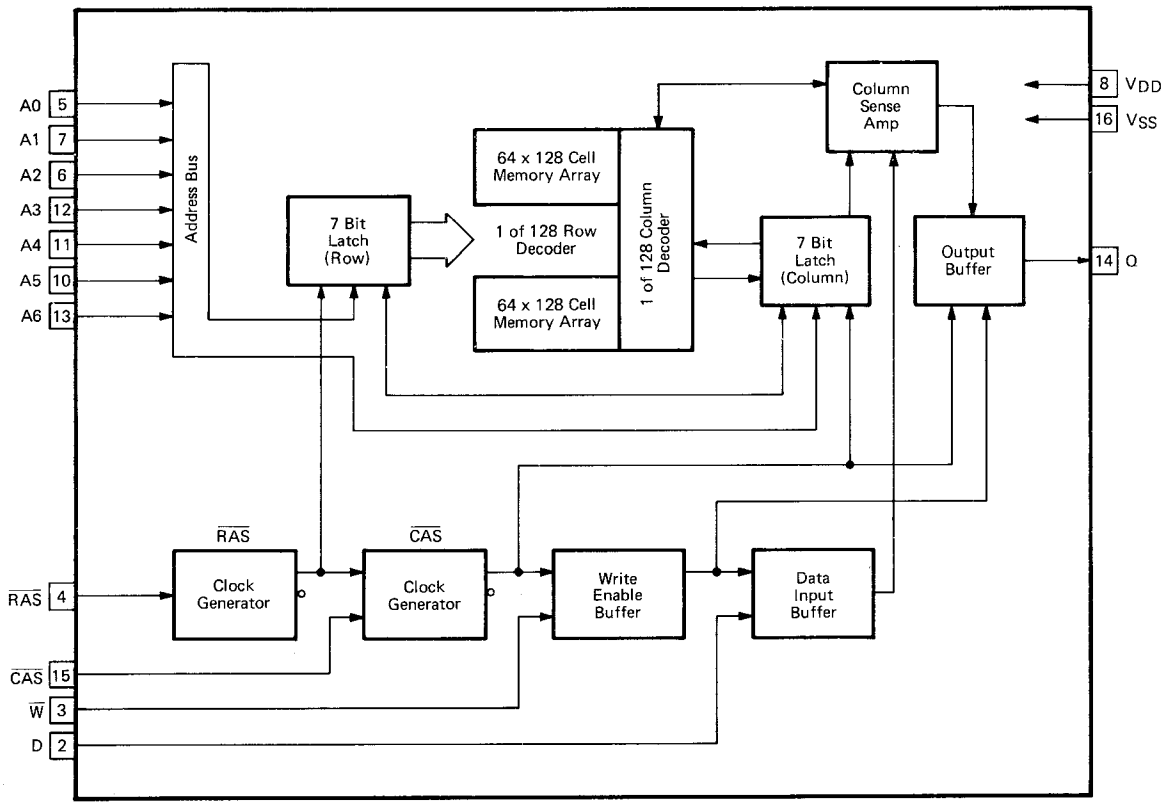
IC11 SN74LS138N (Motorola) or MB74LS138M (Fujitsu) or HD74LS138P (Hitachi)



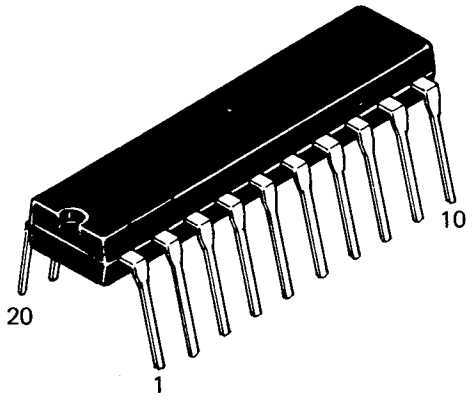
IC14 ~ 21 (64K) MCM6665L20 (Motorola) or HM4864-3 (Hitachi) or MB8264-20P (Fujitsu)

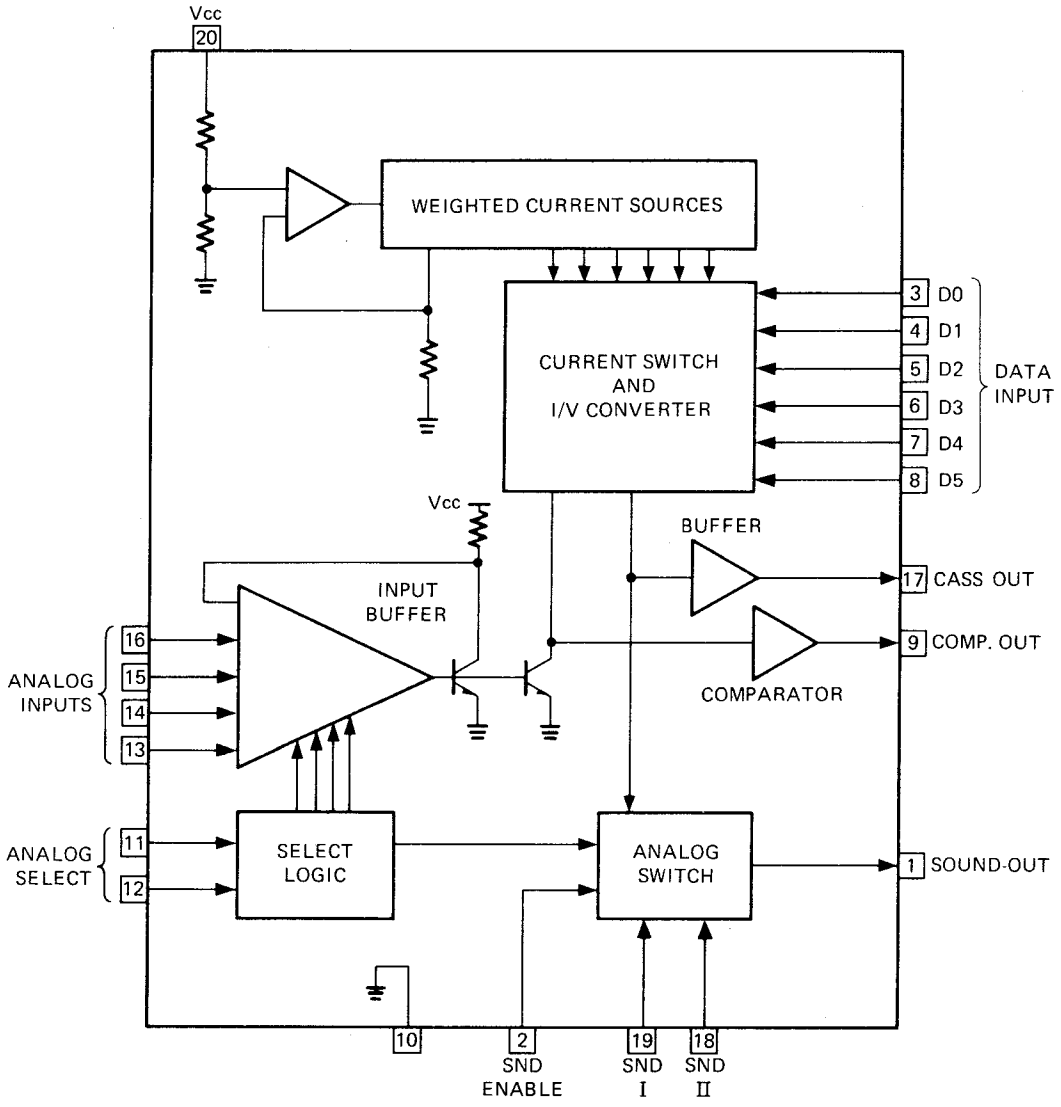


IC14 ~ 21
(16K) MCM4517- (Motorola) or MB8118E (Fujitsu)

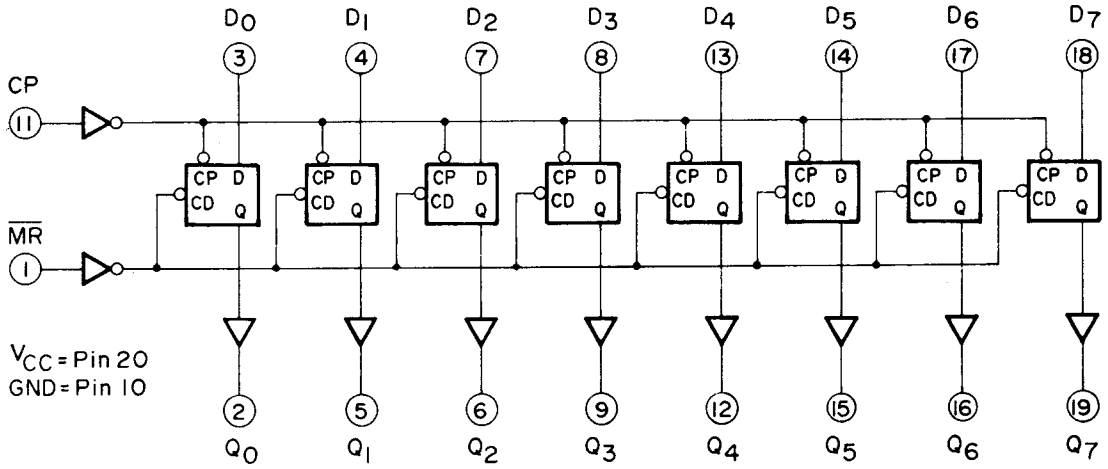


IC3 DAC SC77526P

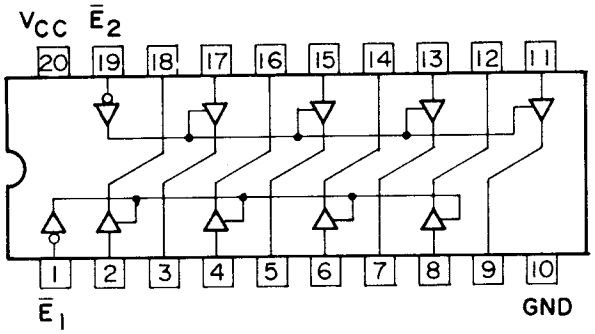




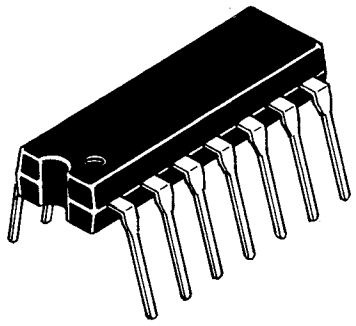
IC5 SN74LS273N (Motorola) or MB74LS273M (Fujitsu) or HD74LS273P (Hitachi)

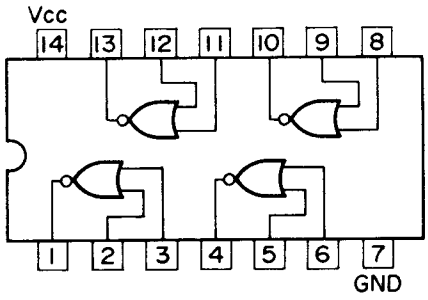


IC6 SN74LS244N (Motorola) or MB74LS244M (Fujitsu) or HD74LS244P (Hitachi)

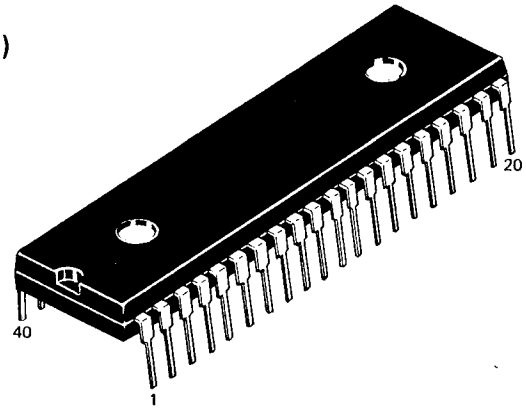


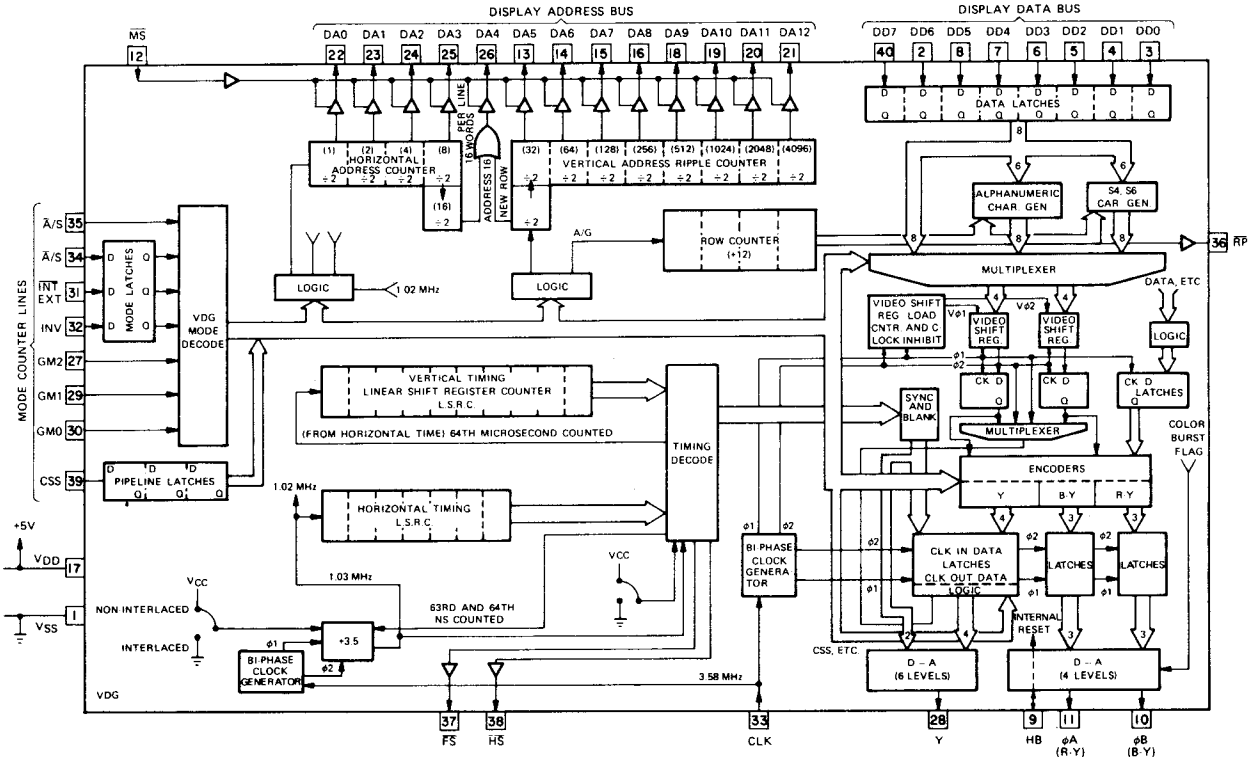
IC10 SN74LS02N (Motorola) or MB74LS02M (Fujitsu) or HD74LS02P (Hitachi)



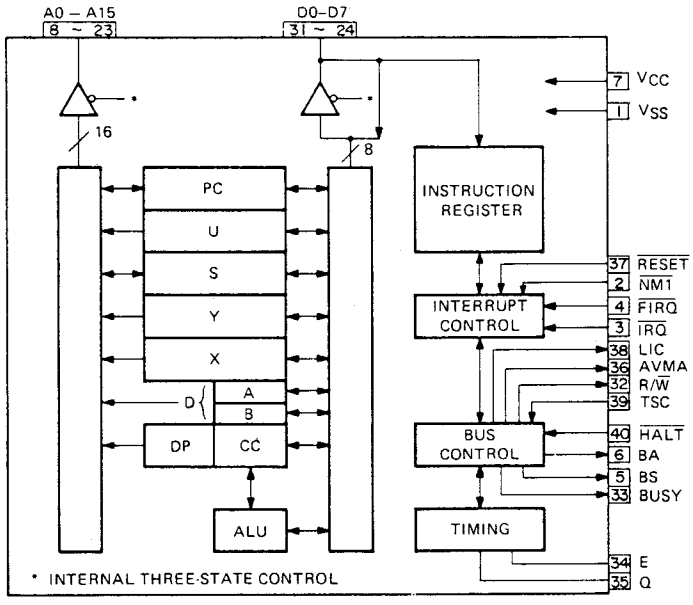


IC8 MC6847P (Motorola)



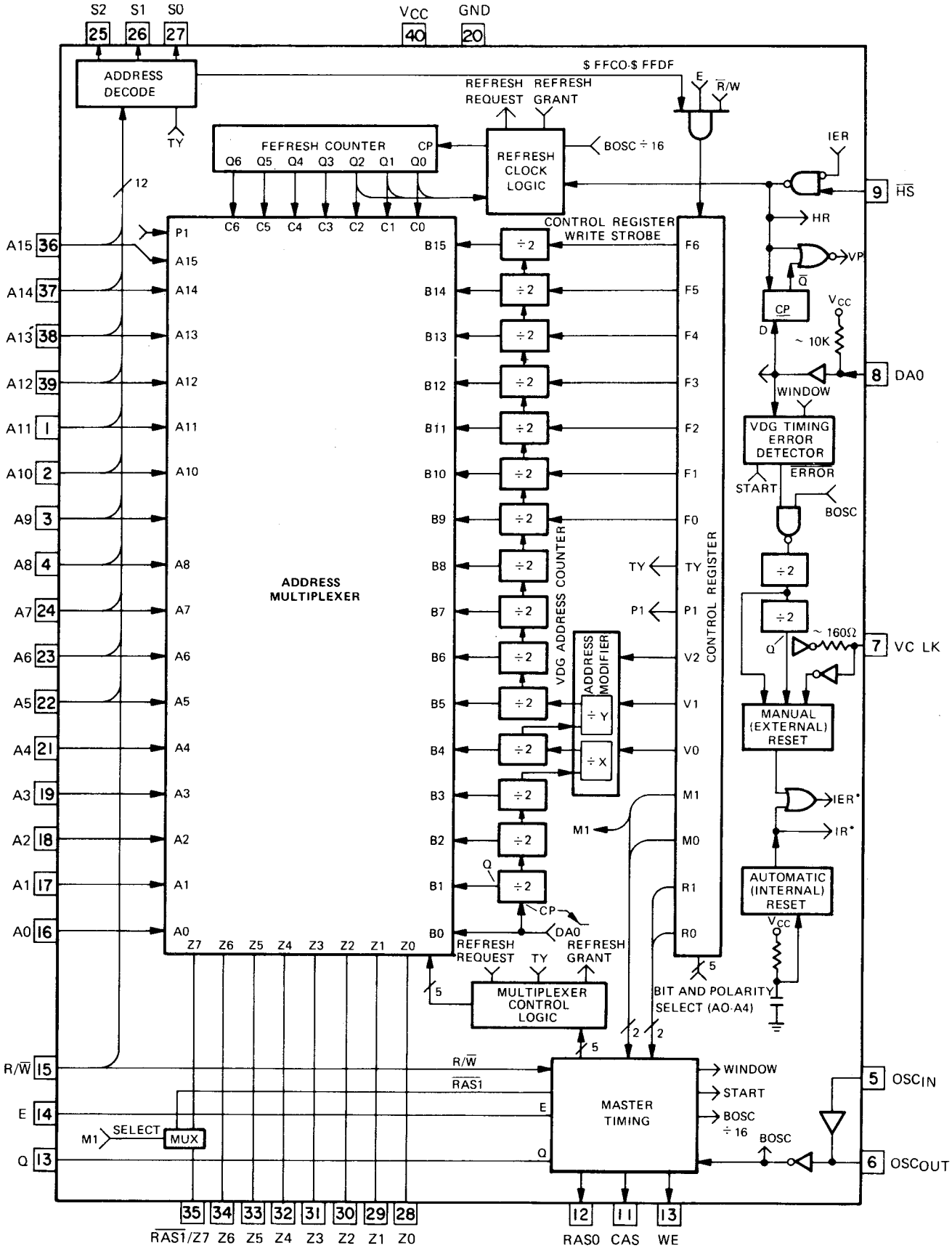


IC9 MC6809EP (Motorola) or HD6809EP (Hitachi)

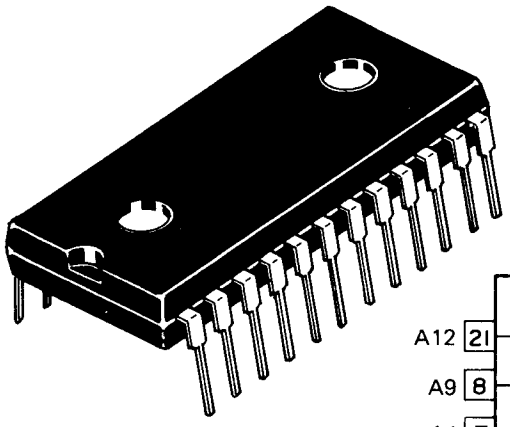


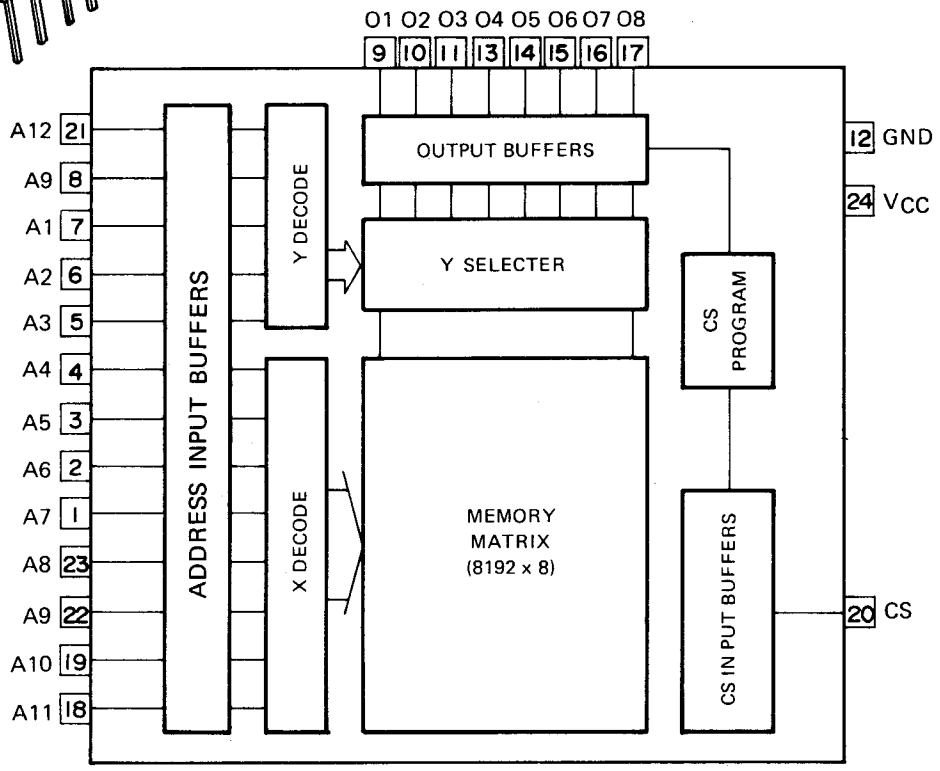
IC2 MC6821P (Motorola) or MBL6821N (Fujitsu) or HD6821P (Hitachi)
IC7 SC67331P (Motorola) —— Refer to Figure 4-12 (page 34)

IC22 SN74LS783 or SN74LS785 (MC6883P) (Motorola)

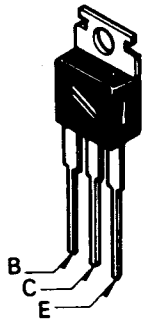


IC12 8040364B (NEC) (Motorola)
IC13 8042364A (NEC) (Motorola)





Q1 2SD 313 D.E
Q2 2SC945



SECTION VII

PARTS LIST

Exploded View Parts List

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
1	Cabinet Assy, Top		AZ7134	M00421
1–1	Cabinet Top	US		601210810A
1–1	Cabinet Top	CA		601210811A
1–2	Plate, Top			711010180A
2	Keyboard		AXX0223	187510200A
3	PCB Assy			20261043TA
	PCB Assy			20261043SA
4	Connector Wire 16P		AJ7567	193910680A
5	Connector Pin		AJ7571	194101351A
6	Modulator MDV-6		AX9471	525010070A
7	Knob Power		AK5012	655000940A
8	Knob Reset		AK5638	659510850A
9	Connector PCB I/O Port		AJ7572	194210060A
10	Holder Connector		AHC2447	411103110A
11	Sheet Shield		AHC2448	473310660A
12	Rivet		AHC2449	HARRA003SN
13	Cover Top Transformer			602310110A
14	Cover Bottom Transformer			602310120A
15	Door I/O Port		ADA0391	603610210A
16	Spring Torsion		ARB7725	434810040A
17	Cabinet Bottom	US	AZ7135	601310690A
	Cabinet Bottom	CA		601310691A
18	Foot with screw		AHC2450	608010060A
19	Holder Reset, Switch		AHC2199	411101870A
20	Socket Assy, Pin		AJ7574	194010410A
21	Spacer Keyboard			852011130A
22	Spacer Keyboard			852011120A
23	Spacer Keyboard			852011040A
24	Spacer Keyboard			852011140A
F1	Screw, TAP TITE, Pan Head 4x25PT-B			
F2	Screw, TAP TITE, Pan Head 4x20PT-B			
F3	Screw, TAP TITE, Pan Head 4x14PT-B			
F4	Screw, TAP TITE, Binding Head 3x8BT-B			
F5	Screw, TAP TITE, Binding Head 2.6x6 BT-B			
F6	Screw, Pan Head 3x10P			
F7	Nut, Flange 3FN			

Electrical Parts List

CAPACITORS								
Ref. No.	Description				DS	RS Part No.	Mfr's Part No.
C1	Electrolytic	220μF	16V	±20%		CC227JDAP	CEACG227M*
C2	Electrolytic	4700μF	16V	±20%		CC478MDAP	CEACG478M*
C3	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL or
	Mylar*	0.1μF	50V	±10%		CC104JJMP	CQQSK104KL
C4	Ceramic	0.022μF	50V	+80–20%		CC223KJCP	CKKPK223Z*
C5	Electrolytic	100μF	16V	±20%		CC107MDAP	CEACG107M*
C6	Ceramic	0.033μF	12V	±30%		CC333NCCP	CGBUF333NT
C7–9	Ceramic	0.022μF	50V	+80–20%		CC223KJCP	CKKPK223Z*
C10	Not Used						
C11/12	Electrolytic	100μF	16V	±20%		CC107MDAP	CEACG107M*
C13/14	Ceramic	0.022μF	50V	+80–20%		CC223KJCP	CKKPK223Z*
C15	Mylar	.0018μF	50V	±10%		CC182JJMP	CQQMK182K*
C16/17	Ceramic	0.022μF	50V	+80–20%		CC223KJCP	CKKPK223Z*
C18	Mylar	.0018μF	50V	±10%		CC182JJMP	CQQMK182K*
C19	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL or
	Mylar	0.1μF	50V	±10%		CC104JJMP	CQQSK104KL
C20	Electrolytic NP/LN	10μF	16V	±20%		CC106MDAP	CEPCG106M*
C21	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL or
	Mylar	0.1μF	50V	±10%		CC104JJMP	CQQSK104KL
C22/23	Ceramic	0.022μF	50V	+80–20%		CC223KJCP	CKKPK223Z*
C24	Ceramic	0.033μF	12V	±30%		CC333NCCP	CGBUF333NT
C25	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL or
	Mylar	0.1μF	50V	±10%		CC104JJMP	CQQSK104KL
C26	Mylar	0.001μF	50V	±10%		CC102KJMP	CQQMK102K*
C27	Ceramic	0.022μF	50V	+80–20%		CC223KJCP	CKKPK223Z*
C28–30	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL
C31	Not Used						
C32	Electrolytic	10μF	25V	±20%		CC106MFAP	CEACI106M*
C33	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL
C34	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL or
	Mylar	0.1μF	50V	±10%		CC104JJMP	CQQSK104KL
C35	Ceramic	0.033μF	12V	±30%		CC333NCCP	CGBUF333NT
C36	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL or
	Mylar	0.1μF	50V	±10%		CC104JJMP	CQQSK104KL
C37	Cer SL	62pF	50V	±5%		CC620JJCP	CCJVK620J*
C38/39	Cer SL	56pF	50V	±5%		CC560JJCP	CCJVK560J*
C40	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL
C41/42	Not Used						
C43/44	Cer NPO	24pF	50V	±5%		CC240JJCP	CCJBK240J*
C45	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL
C46	Electrolytic	10μF	25V	±20%		CC106MFAP	CEACI106M*
C47	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL
C48	Electrolytic	1μF	50V	±20%		CC105KJAP	CEACK105M*
C49	Not Used						
C50/57	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL
C58	M-Plastic	0.1μF	50V	±5%		CC104JJYP	CFQMK104JL or
	Mylar	0.1μF	50V	±10%		CC104JJMP	CQQSK104KL

*Mylar is a registered trademark of E.I. Du Pont de Nemours and Company.

Ref. No.	Description				DS	RS Part No.	Mfr's Part No.
C59	Cer SL	150pF	50V	±5%		CC151JJCP	CCJVK151J*
C60	Not Used						
C61	Cer SL	150pF	50V	±5%		CC151JJCP	CCJVK151J*
C62	Electrolytic	22μF	16V	±20%		CC226KDAP	CEACG226M*
C63/66	Ceramic	0.01μF	50V	+80—20%		CC103JJCP	CKKPK103Z*

TRIMMER CAPACITOR

Ref. No.	Description		DS	RS Part No.	Mfr's Part No.
TC1	Trimmer,	6 ~ 50pF		AC0988	154010240A

DIODES

Ref. No.	Description			DS	RS Part No.	Mfr's Part No.
D1/2	Silicon	1N4002	Rectifier		DX0206	SDSI00036- or
	Silicon	SR1K-2				SDSI00026- or
	Silicon	10E1			DX1039	SDSI00003- or
	Silicon	1N4002			DX0206	SDSI00007-
D3/4	Silicon	30D1	Rectifier		DX2321	SDSI00059- or
	Silicon	GP30B				SDSI00061- or
	Silicon	G3B				SDSI00078-
D5/6	Zener	RD3.9E-B	Protector		DX2323	SZRD3.9EB- or
	Zener	GZA3.9 (Y)				SZGA3.9—Y or
	Zener	UZ-3.9				SZUZ3.9— or
	Zener	RD3.9EN-				SZRD3.9EN- or
	Zener	RD3.9E-L				SZRD3.9EL-
D7/8	Germanium	1KF20-04	Switching		DX2322	SDGE00012-
D9-12	Silicon	1S953	Switching		DX2327	SDSI00015- or
	Silicon	1N4148			DX0022	SDSI00057- or
	Silicon	1N4148			DX0022	SDSI00064-
D13	Germanium	1KF29-04	Switching		DX2322	SDGE00012-

ICS

Ref. No.	Description			DS	RS Part No.	Mfr's Part No.
IC1	8050527 (SC77527P)		Bipolar SALT		MX6201	SISC50527-
IC2	MC6821P	N-MOS	PIA		AMX4578	SIMC#0004- or
	MBL6821N					SIMB#0004- or
	HD6821P					SIHD#0004-
IC3	8050526 (SC77526P)	C-MOS	DAC		MX6202	SISC50526-
IC4	NJM555D	Linear	Timer		MX5741	SINM555D— or
	NE555P				AMX3652	SIIE555P—

Ref No.	Description	DS	RS Part No.	Mfr's Part No.
IC5	SN74LS273N TTL Latch MB74LS273M HD74LS273P		AMX4227	SIRNS273N- or SIMBS273M- or SIHDS273P-
IC6	SN74LS244N TTL Buffer MB74LS244M HD74LS244P		AMX3864	SIRNS244N- or SIMBS244M- or SIHDS244P-
IC7	SC67331P N-MOS PIA Select		MX6211	SISC67331-
IC8	MC6847P N-MOS VDG		AMX4575	SIMC6847P-
IC9	MC6809EP N-MOS CPU HD6809EP HD68A09EP		MX5560	SIMC#0003- or SIHD#0003- or SIHD#0003A
IC10	SN74LS02N TTL Nor-Gate MB74LS02M HD74LS02P		AMX3551	SIRNS02N– or SIMBS02M– or SIHDS02P–
IC11	SN74LS138N TTL Decoder MB74LS138M HD74LS138P		AMX4583	SIRNS138N- or SIMBS138M- or SIHDS138P-
IC12	8040364B ROM BASIC 8040364B (μPD236C-1)		MX6203	SISC40364B or SITN40364B
*IC13	8042364A ROM Extend 8042364A (μPD2364C-1)		MX6200	SISC42364A or SITN42364A
IC14–21	MB8118-12P Memory MCM4517-20 MCM4517P-15		MX6199	SIMB#0006- or SICM4517-2 or SICM4517PF
IC22	74LS783 TTL SAM 74LS785		MX6198	74LS783 or 74LS785

*For 26-3136 only

JACKS

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
JK1/2	DIN Joystick DIN		AJ7566	193410040A or 193410070A
JK3	DIN RS232C DIN		AJ7357	193410020A or 193410050A
JK4	DIN Cassette DIN		AJ7356	193410030A or 193410060A

COIL

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
L1	Inductor 100μH Inductor 100μH		ACA8339	142011510A or 142000801A

TRANSISTORS

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
Q1	2SD313 (E) NPN Regulator		2SD526	ST2D313–E or
	2SD313 (F)			ST2D313–F or
	KTD880 (Y)			STKD880–Y or
	KTD880 (GR)			STKD880–G
	2SC945 (P) NPN Switching		2SC945	ST2C945–P or
	2SC536K (G)		2SC536	ST2C536K–G

Resistors

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
R1	Carbon 51 ohm 1/4W ±5%		N0103EEC	RCSQP510J*
R2	M-Film 0.1 ohm 1W ±5%		N0001EGE	RMO1HR10J*
R3	Carbon 270 ohm 1/2W ±5%		N0155EFC	RCSHP271J*
R4	Carbon 510 ohm 1/4W ±5%		N0173EEC	RCSQP511J*
R5/6	Carbon 4.7Kohm 1/4W ±5%		N0247EEC	RCSQP472J*
R7/8	Carbon 10Kohm 1/4W ±5%		N0281EEC	RCSQP103J*
R9	Carbon 1.0Kohm 1/4W ±5%		N0196EEC	RCSQP102J*
R10	Carbon 9.1Kohm 1/4W ±5%		N0276EEC	RCSQP912J*
R11	Carbon 100 ohm 1/2W ±5%		N0132EFC	RCSHP101J*
R12	Not Used			
R13	Carbon 10Kohm 1/4W ±5%		N0281EEC	RCSQP103J*
R14	Carbon 4.7Kohm 1/4W ±5%		N0247EEC	RCSQP472J*
R15	Carbon 1.5Kohm 1/4W ±5%		N0206EEC	RCSQP152J*
R16	Carbon 10Kohm 1/4W ±5%		N0281EEC	RCSQP103J*
R17/18	Carbon 4.7Kohm 1/4W ±5%		N0247EEC	RCSQP472J*
R19	Carbon 100 ohm 1/4W ±5%		N0132EEC	RCSQP101J*
R20	Carbon 100Kohm 1/4W ±5%		N0371EEC	RCSQP104J*
R21	Carbon 4.7Kohm 1/4W ±5%		N0247EEC	RCSQP472J*
R22	Carbon 100Kohm 1/4W ±5%		N0371EEC	RCSQP104J*
R23	Carbon 220 ohm 1/2W ±5%		N0149EFC	RCSHP221J*
R24	Carbon 100 ohm 1/4W ±5%		N0132EEC	RCSQP101J*
R25	Carbon 150 ohm 1/4W ±5%		N0142EEC	RCSQP151J*
R26	Carbon 100 ohm 1/4W ±5%		N0132EEC	RCSQP101J*
R27/8	Carbon 4.7Kohm 1/4W ±5%		N0247EEC	RCSQP472J*
R29/30	Carbon 1.0Kohm 1/4W ±5%		N0196EEC	RCSQP102J*
R31	Carbon 2.2Kohm 1/4W ±5%		N0216EEC	RCSQP222J*
R32/33	Carbon 33 ohm 1/4W ±5%		N0087EEC	RCSQP330J*

RELAY

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
RY1	Relay		AR8166	581010140A or 581010160A

SWITCHES

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
SW1	Push Power		AS2900	182110240A
SW2	Key Reset		AS2849	187010040A
SW3	Slide Channel		AS2847	183110240A

TRANS.

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
T1	Power	US	ATA1056	10101163DA
	Power	CA		10101164DA

CRYSTAL

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
X1	14.31818MHz		MX1112	391010720A

MISCELLANEOUS

Ref. No.	Description	DS	RS Part No.	Mfr's Part No.
	Socket, IC 40P		AJ7568	195110200A or
	Socket, IC 40P			195110280A
	Socket, IC 24P		AJ7569	195110180A
	Socket, IC 24P			195110260A
	Socket, IC 16P		AJ7570	195110140A or
	Socket, IC 16P			195110240A
	Cord Patch		AW3222	313510110A or
	Cord Patch			313510130A
	Box Switch		AX9472	189510030A or
	Box Switch			189510040A

SECTION VIII

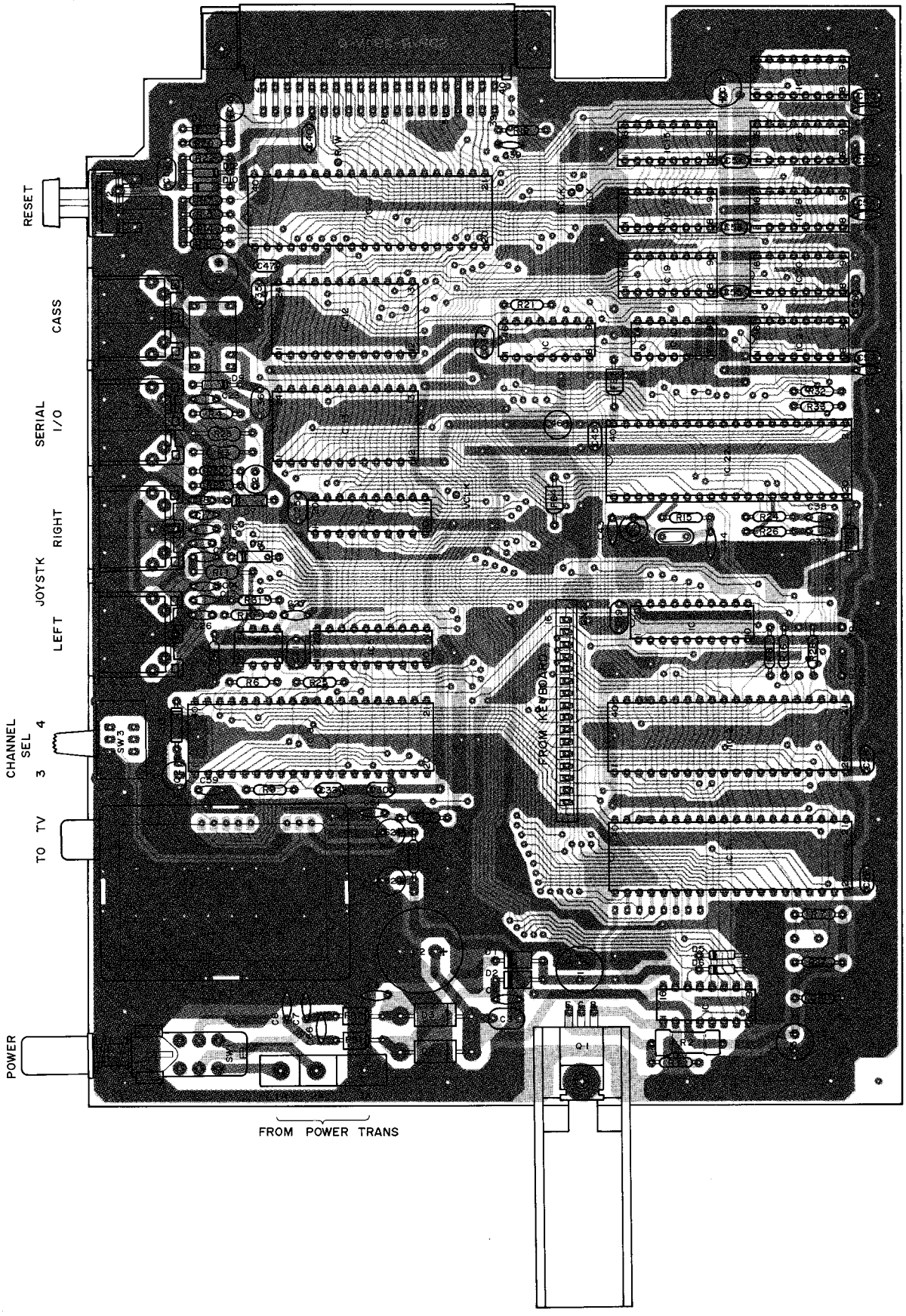
SCHEMATIC DIAGRAM

SECTION IX

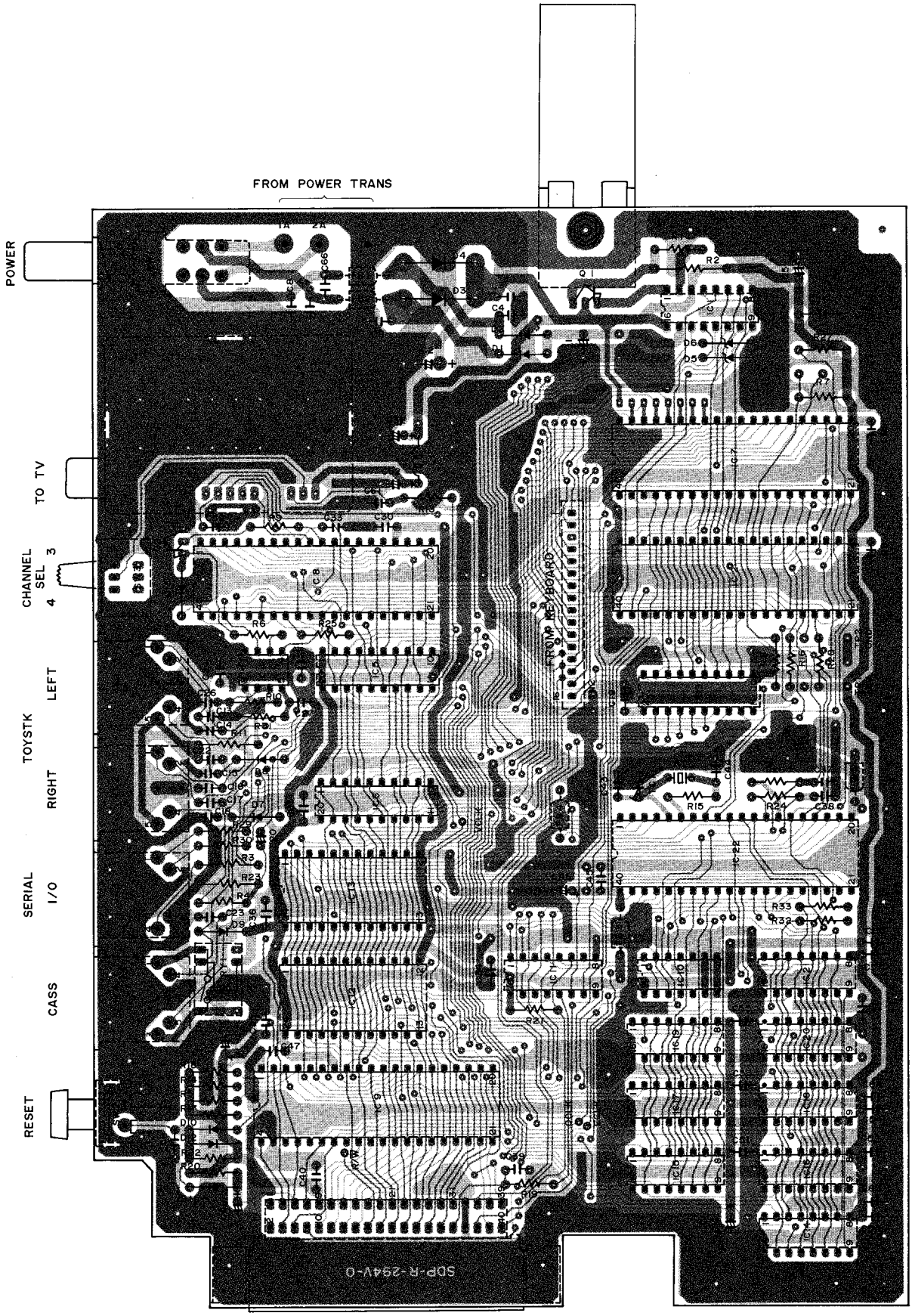
P.C.B. VIEWS

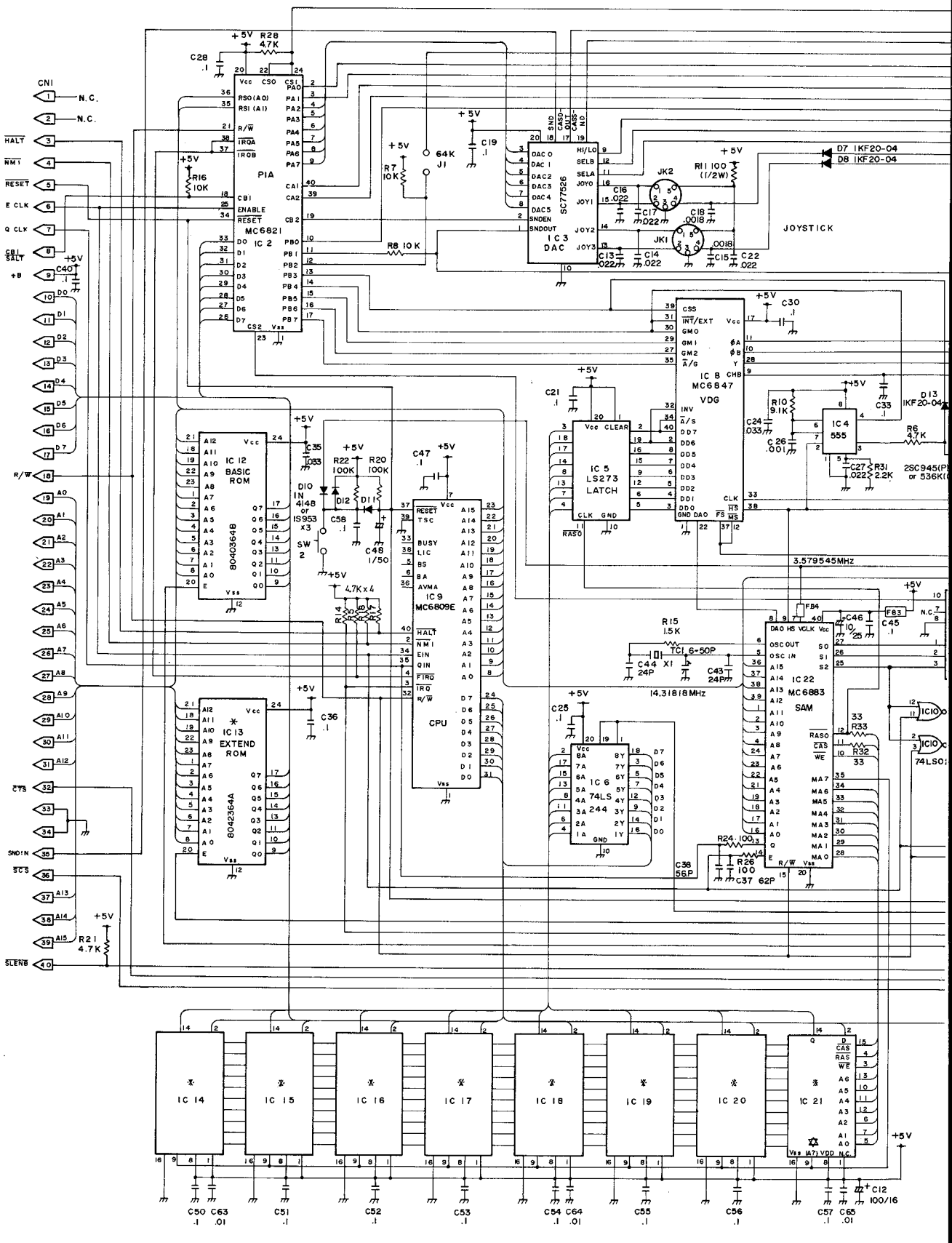
Main P.C.B.

Top View

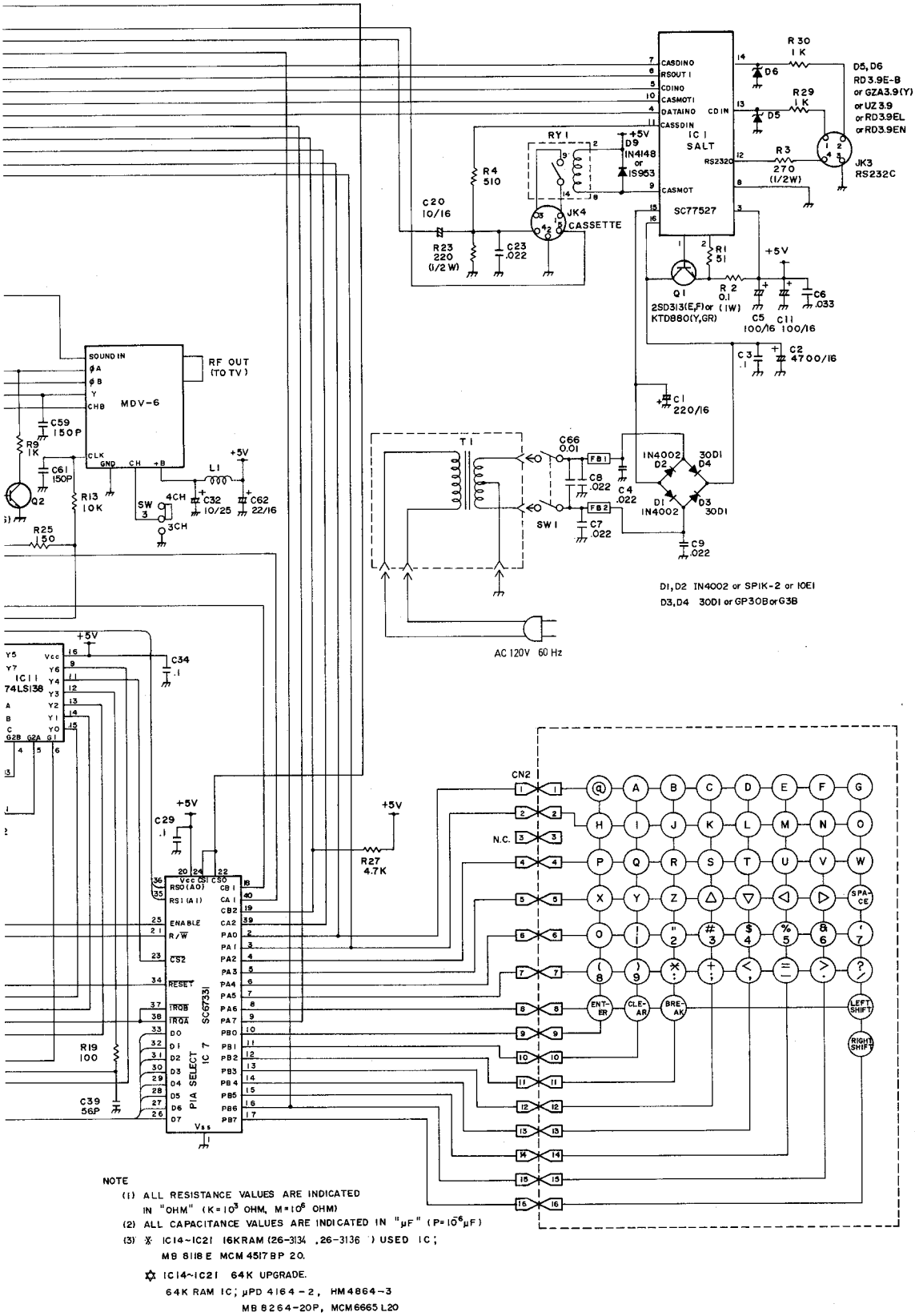


Bottom View


FROM POWER TRANS
POWER
TO TV
CHANNEL SEL 3 4
TOYSTK LEFT RIGHT
SERIAL I/O CASS
RESET
FROM KEYBOARD
SDP-R-2544V-0


CN1
N.C.
N.C.
HALT
NMI
RESET
E CLK
Q CLK
CBI SALT
+B
R/W
CTS
SND IN
SCS
SLENB
PIA
MC6821
IC 2
IC 3 DAC
SC77526
JOYSTICK
JK1
JK2
64K J1
D7 IKF20-04
D8 IKF20-04
IC 8 CHB
MC6847
VDG
IC 4
555
IC 5
LS273
LATCH
IC 12
BASIC ROM
IC 13
EXTEND ROM
CPU
IC 9
MC6809E
IC 22
MC6883
SAM
IC 6
74LS 244
3.579545MHz
14.31818MHz
IC 14
IC 15
IC 16
IC 17
IC 18
IC 19
IC 20
IC 21

IAGRAM



NOTE

(1) ALL RESISTANCE VALUES ARE INDICATED IN "OHM" (K=10^3 OHM, M=10^6 OHM)

(2) ALL CAPACITANCE VALUES ARE INDICATED IN "μF" (P=10^{-6}μF)

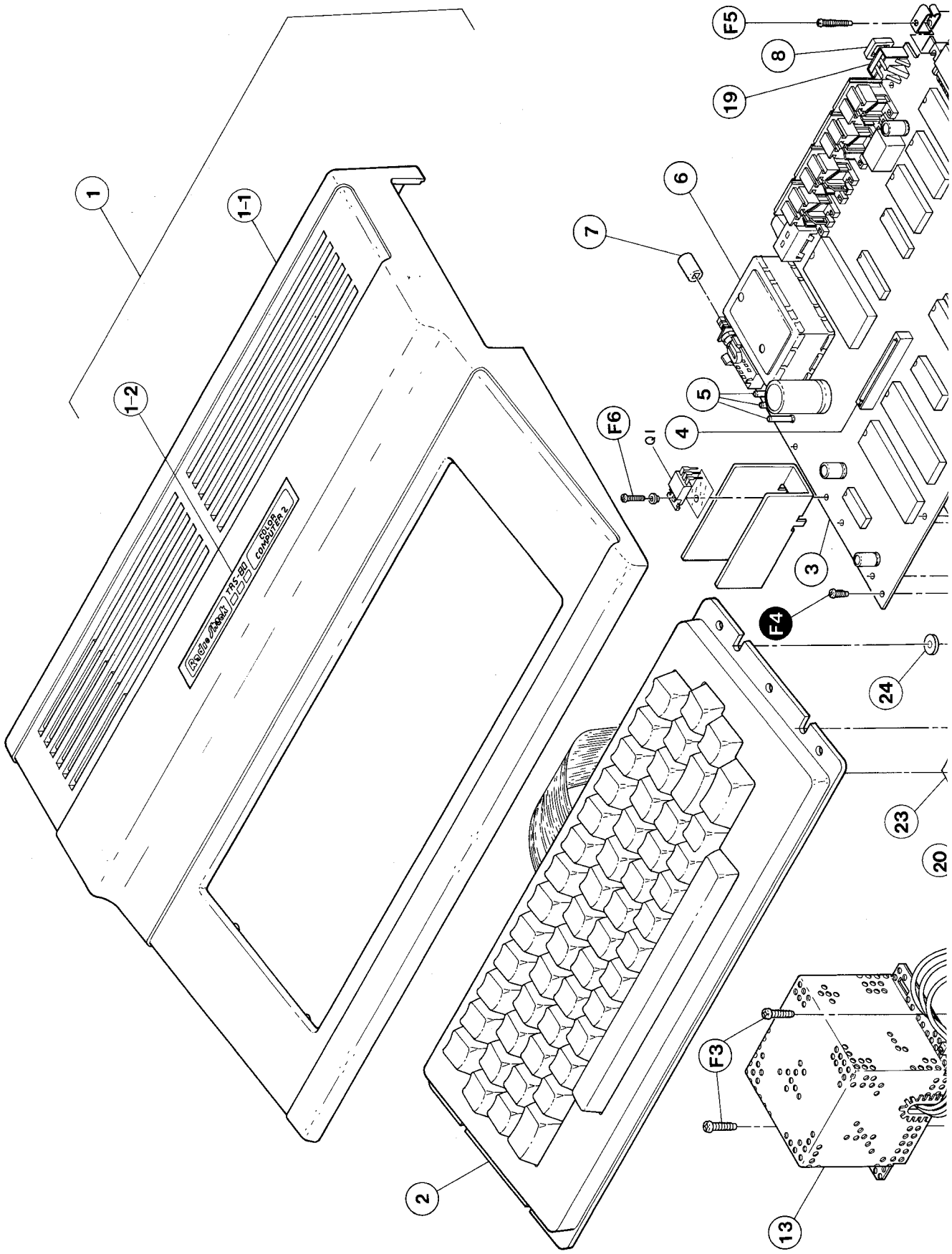
(3) ※ IC14~IC21 16KRAM (26-3134 ,26-3136) USED IC;
MB 8118E MCM 4517 8P 20.

✡ IC14~IC21 64K UPGRADE.
64K RAM IC; μPD 4164-2, HM4864-3
MB 8264-20P, MCM6665 L20

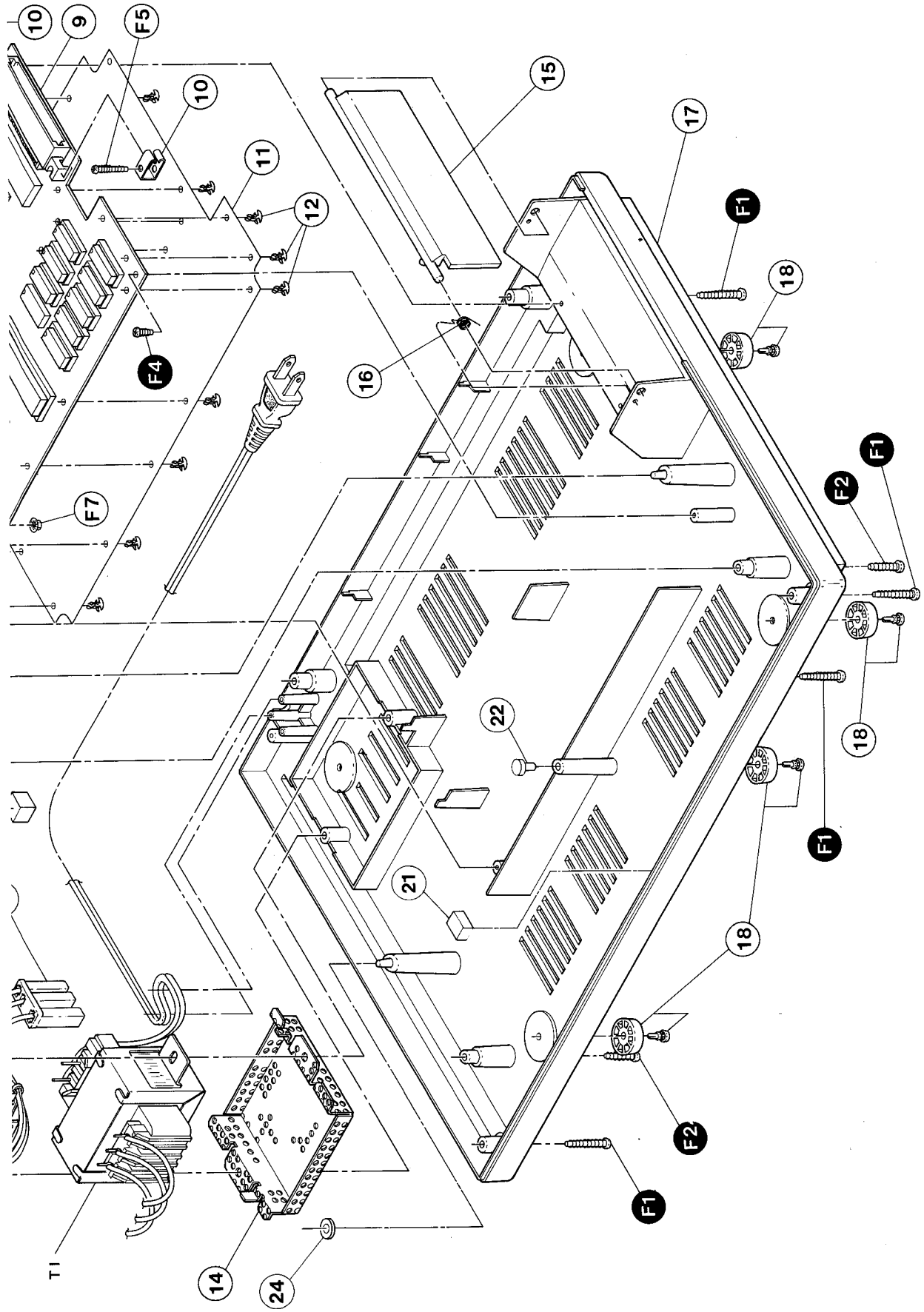
SECTION X

EXPLODED VIEW

EXPLODED



VIEW



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