PIPELINES

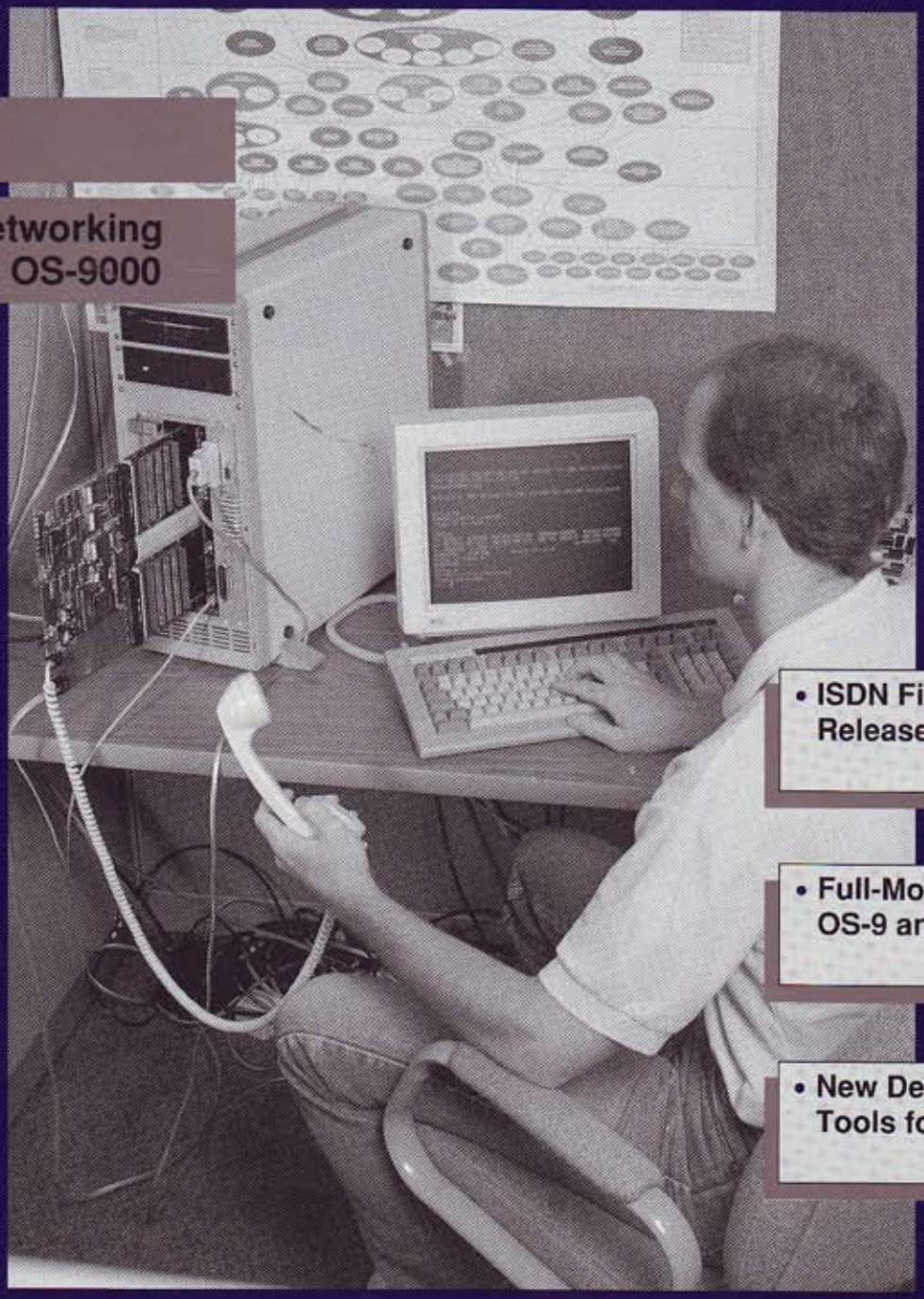
Volume 7 Number 4

Covering Microware's Real-Time System Solutions

Fall 1992

ISDN:

Wide Area Networking For OS-9 and OS-9000



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PIPELINES

Fall 1992
Volume 7 Number 4

PIPELINES is published quarterly by:
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ISDN engineer Curt Schwaderer tests the Terminal Adapter Microware Interface (TAMI) board designed by Microware.

New Products for the New Year

Ken Kaplan
Microware's President

WE'RE WINDING UP A VERY EXCITING AND eventful 12 months here at Microware. We started out 1992 celebrating our 15th anniversary, and we're finishing up the year by rolling out more new products. We've already released Ultra C, our advanced technology ANSI C compiler, and a new version of OS-9000 that allows real time, DOS and Windows to share the same environment.

And, now it gets even better. This issue of *PIPELINES* is literally packed with new offerings. Our ISDN and full-motion video products bring Microware's real-time system software to the heart of digital multimedia and telecommunications systems around the world. This issue also features two new development tools for OS-9000

NEW PRODUCT

ISDN: Bringing Wide Area Networking to OS-9 and OS-9000

by Curt Schwaderer
Microware Systems Corporation

THE INTEGRATED SERVICES DIGITAL NETWORK, or ISDN, is a single telecommunication network designed to service a wide variety of needs. ISDN's main focus is to support a wide range of integrated voice and non-voice applications over the same network by providing a standardized protocol for worldwide networking interconnectivity.

Microware has developed the **ISDN File Manager (ISM)** for both OS-9 and OS-9000. ISM is the pilot product in Microware's commitment to providing worldwide network connectivity for the OS-9 and OS-9000 operating systems.

ISM provides Basic Rate ISDN support for use in WAN and telecommunications products. These products might include video conferencing systems, high-speed fax machines, LAN/WAN bridges and routers, and other network applications.

ISDN is designed to integrate a set of services, including voice, data and video, over a standardized digital telephone system. The existing telephone system pro-

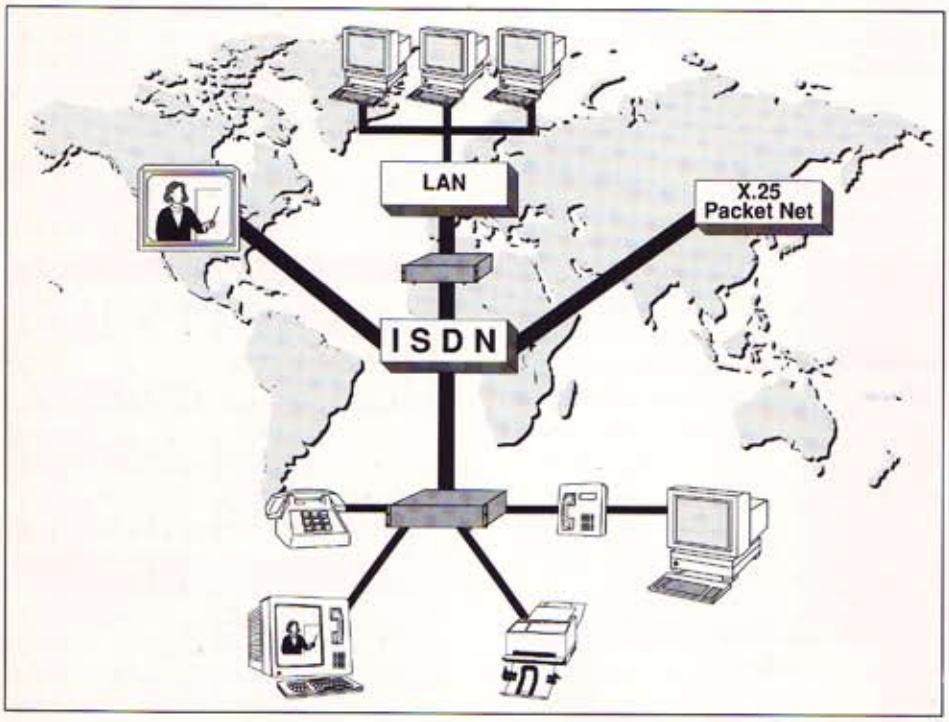
that provide designers even more flexibility for developing real-time applications built around 386/486 hardware platforms. And you'll find an expanded "New Vendor Products" section that highlights new software and hardware offerings for both OS-9 and OS-9000.

Take a look at our "New Faces at Microware" page and our "Microware Around The World" section. You'll see how Microware is continuing its strong growth in terms of new employees and an expanding distributor network.

But it doesn't stop there; we are ready to blast into 1993 with even more products. In the coming months, we'll be releasing a new cross development package that will set the industry standard for functionality and versatility. Plus, we'll be introducing specialized and cost-effective software for embedded systems development that will speed products to market. And we'll continue to develop multimedia and wide area networking tools that will bring Microware's system software into virtually every home in the world.

I'd like to give you a peak at some of the "goodies" that our development groups are working on, but the R&D gang just won't let me say any more. I can guarantee you one thing, Microware will be the real-time system software developer to watch in 1993.

— Ken Kaplan



ISDN opens a world of possibilities for wide area networking and telecommunications. The protocol holds possibilities for high-speed fax machines, LAN/WAN bridges and routers, and video conferencing.

vides some digital switching capabilities, but is far from being a "digital network."

Our Current Telephone System

The existing system is really an analog system with digital switches. A message travels through the system as analog data until it reaches a switch. The switch digitizes the message and routes it toward the next point. The message is then translated back to analog data and travels along the telephone lines to the next switch. This con-

Wide Area Networking
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NEW PRODUCT

OS-9/MVME147 Now Includes BootP Support

AN UPDATE TO OS-9 FOR THE MVME147 INCLUDES client and server support for the BootP network booting protocol, as well as system and utility enhancements.

MVME147 BootP Overview

BootP is a client-server protocol where an OS-9 client makes a request to a server system across the network. The server then identifies the client and transfers an OS-9 bootfile across the network to the client.

The BootP option is started by the OS-9 ROM boot code, either through a menu selection or automatically with no operator intervention. The client will read the OS-9 bootfile as it is transferred across the network and copy it into local RAM in the same manner as other boot device drivers.

This update of OS-9 for the MVME147 includes client BootP support for the on-board LANCE chip set and the MVME374 Ethernet controller board. Server BootP support is provided for the on-board LANCE chip set only.

Now Available

In addition to added support for BootP, the **OS-9/MVME147** update includes the latest shipping versions of system modules and utilities. The updated OS-9/MVME147 Development Pak is now available. Contact Microware or your authorized Microware representative to order your Development Pak, upgrade existing products or for more information. MSC

OS-9 for Motorola's MVME147 single board computer now includes BootP support.

NEW PRODUCT

Full-Motion Video for OS-9 and OS-9000 Systems

The Motion Picture File Manager (MPFM) provides MPEG full-motion video support for OS-9 or OS-9000 systems.

THE MPEG (MOTION PICTURE EXPERTS Group) standard for full-motion video specifies advanced compression and decompression methods for video and audio files. MPEG can be used in applications ranging from CD-based karaoke, CD-ROM XA and video-on-demand systems, to point-of-information systems and automatic teller machines. Microware announces the release of the Motion Picture File Manager (MPFM) for support of this worldwide standard.

MPFM is a drop-in I/O extension for the OS-9 and OS-9000 Real-Time Operating Systems that supports real-time playback of MPEG encoded audio and video files. Users can now play back full-screen, full-motion video complete with synchronized digital audio. MPFM is fully-compatible with the MPEG file manager used with compact disc-interactive (CD-I) systems.

MPFM supports world standard audio and video formats and provides options for playback control. Video can be configured to play back in a variety of display environments, including windowing, with full control of playback rates for scan, freeze, slow motion and step frame. Audio control provides volume control, stereo panning and muting.

MPFM Architecture

MPFM is a dual-ported file manager written in C to accommodate OS-9 systems on Motorola 68XXX platforms and OS-9000 systems operating with 386/486 microprocessors. Like all Microware file managers, MPFM is 100 percent ROMable and can be easily added to any existing OS-9 or OS-9000 system.

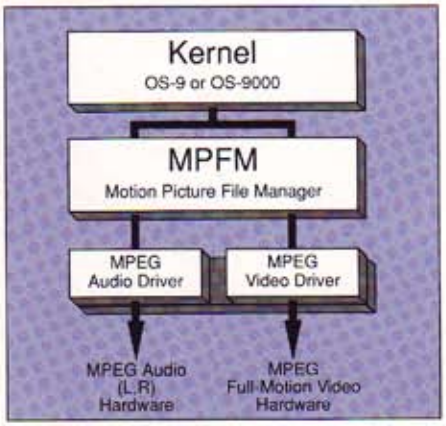
Working example MPEG audio and video drivers are included to support playback on standard sound equipment and color monitors.

The Moving Picture Experts Group

The Moving Pictures Expert Group is a consortium of experts from the computer, telecommunication, consumer electronic and broadcasting industries to specify and standardize digital motion picture media. The resulting MPEG specification is a worldwide standard which encompasses encoding, decoding and playback of motion picture sound and video images. The MPEG standard is hardware- and software-independent allowing MPEG files to be played back on a variety of multimedia systems including OS-9, OS-9000 and CD-RTOS.

MPEG File Stream

The MPEG file stream consists of encoded video and audio packets multiplexed into multiple streams. MPFM supports up to 16 MPEG video and 32 MPEG audio streams. Either the MPFM device drivers or the MPEG hardware can demultiplex the streams. Channel switching during playback is supported at the application level for both audio and video channel switching.



Schematic of the Motion Picture File Manager (MPFM) for OS-9 and OS-9000.

MPFM supports MPEG decoding data rates at 1.2M/sec. to 6M/sec. MPFM supports 24, 25 and 30 frames per second for NTSC- and PAL-compatible display systems.

Audio and Video Synchronization

Sequenced audio and video may be played either independently or in a synchronized manner. Several requests can also be queued to sequentially play upon completion of the previous sequence.

Adding MPFM to Your Multimedia System

MPFM for OS-9 can be added to any Motorola 68XXX-based system supporting OS-9 Version 2.4 (or greater), or any OS-9000 Version 1.3 (or greater) 386/486 system equipped with C Cube's PC/AT MPEG board.

MPFM is available in OEM installation source code packages for OS-9 licensees and single, non-transferable object code copy packages for OS-9000 PC/AT end users.

To add MPEG support to your system or for more information, contact Microware or your authorized Microware representative. MSC

NEW PRODUCT

Character-Based Graphical Interfaces with OS-9000/QD MenuMaker

MICROWARE'S **OS-9000 QD MENUMAKER** provides a tool with which to develop character-based graphical user interfaces on 386/486 systems running OS-9000. OS-9000/QD MenuMaker provides a library of screen functions for ***Draw***, ***Terminal Capabilities I/O (TCIO)*** and ***Menu*** control. OS-9000/QD MenuMaker's screen editor is a full-color graphic editor that works with the screen library to provide a method to develop interfaces for use in user applications.

Interfaces created under QD MenuMaker can be used to monitor and interact with OS-9000 processes, provide a graphical representation of applications, and include interactive menu and help screens in applications.

The screen editor works in text mode on the monitor connected to an OS-9000 386/486 system and uses pseudo-graphic characters from the extended ASCII code table to draw and fill boxes.

Draw functions place objects on the screen. ***TCIO*** functions build on the ***Draw*** functions and, together with the ***termcap*** library, provide cursor motion and allow input from the keyboard. ***Draw*** and ***TCIO*** functions are combined by the ***Menu*** functions to create pull down and bar-style menus.

OS-9000/QD MenuMaker provides a function library and tools for developing character-based graphical interfaces.

QD MenuMaker's color palette can be accessed in two different ways. First, the ***palette*** program graphically displays the palette and lets users select the colors to be used. Second, the use of the ***palette()*** functions allows palette register assignment to be handled directly by the application.

QD MenuMaker is designed to be installed on a disk-based 386/486 system running Professional OS-9000 Version 1.3 or greater. QD MenuMaker also requires either a VGA or EGA graphics adapter for the 386/486 system.

Ordering QD MenuMaker

To order QD MenuMaker for OS-9000 386/486 systems or for more information, contact Microware or your authorized Microware representative. MSC

NEW PRODUCT

POLYTRON Version Control System for OS-9000

THE **OS-9000 POLYTRON VERSION CONTROL SYSTEM (PVCS)** is a complete source code control system for software project management. The package consists of ten integrated program modules that provide complete control over the evolution of a software development project. In addition, OS-9000/PVCS provides support for Ultra C, Microware's ANSI C compiler.

A "logfile" that contains descriptions, current revisions and a complete history of modifications is created for each project. Each logfile can include program source code, object code, libraries or project documentation.

Project management is provided through the ability of individual users to "check out" selected logfiles, make modifications, and then "check in" the file with a description of modifications.

OS-9000/PVCS provides extensive control over user access to the logfile and associated workfiles. File access can be assigned to individuals or groups. PVCS also allows the definition of which PVCS functions can be used by individual users. This allows the project manager to specifically assign accessibility to users based on their activities.

```
$ pvdiff old_test.c test.c
   old_test.c (09 Nov 1992 11:04:00)
         test.c (17 Nov 1992 15:34:00)
------------------------------------------------------------------------
     321     321          /* check all cop>= */
     322     322          check_assign_ops();
+            323          check_assign_ops_again();
     323     324
     324     325          /* write final cemetery */
------------------------------------------------------------------------
     353     354     while (cemetery) {
     354     355          set_free(cemetery->ref_set);
+            356          cemetery = cemetery->prev;
     355                  cemetery = cemetery->next;
     356     357     }
     357     358
------------------------------------------------------------------------
     363     362     set_free(effected);
     364     363     set_free(old_volatile);
> (  359)   364
> (  360)   365     que_free(work);      /* release the allocated queue */
     365     366
     366     367     block_term(ref_node_block); /* get rid of ref_node */
------------------------------------------------------------------------
$
```

Sample OS-9000/PVCS screen showing the use of the *pvdiff* module. Here, the differences between *old_test.c* and *test.c* are displayed.

PolyMake Included

OS-9000/PVCS also includes PolyMake, an enhanced ***make*** facility that automates the task of building programs from their source components.

OS-9000/PVCS is designed to be installed on a disk-based 386/486 system running Professional OS-9000 Version 1.3 or greater.

Ordering PVCS for OS-9000

To order PVCS for OS-9000 386/486 systems or for more information, contact Microware or your authorized Microware representative. MSC

Development of the BVME390: A Case Study

by David Smith
BVM Limited
Southampton, England

TWO FUNDAMENTAL, CRITICAL CRITERIA WERE defined when the decision to develop the 3U VMEbus BVME390 68040-based CPU board was taken by BVM:

- The new board had to be fully backwards compatible with boards based on previous 680X0 processors, allowing users a straightforward migration path
- The board had to take full advantage of the new 68040 features, so as to offer a significant performance upgrade

The unit was also designed from the start to run OS-9, as are all BVM products.

Porting OS-9 to the BVME390 was simplified in some ways because existing peripheral drivers could be used with minor modifications. However, the complexity and intrinsic capability of the 68040 meant that it was by no means an easy task to optimize the board's performance.

It is impossible to optimize a board design for all operating systems, hence the benefit of having a long-term, close relationship between the hardware and software designers.

As the design proceeded, it became more and more obvious that in order to achieve our goals, a number of software/hardware interface problems had to be resolved at the board design level. This in turn meant that there had to be considerable two-way dialog between BVM and Microware. So close was this dialog that BVM's suggestions served as the foundation for some of the upgrades to OS-9. The main conclusion to be drawn from the BVM experience is that it is impossible to optimize a board design for all operating systems, hence the benefit of having a long-term, close relationship between the hardware and software designers.

Caching Issues

The issue of cache compatibility was the major area which had to be addressed.

The 68040, which has 4K instruction and data caches, presented a significant problem, a problem exacerbated by the fact that the caching mechanism can be either write-through, or copyback. In write-through caching, the CPU only updates the cache on data writes, thereby achieving maximum bandwidth. With copyback caching, data may remain in the cache and stale data remains in the main memory. In this case a DMA device could access stale main memory data, leading to system problems.

In a software solution to handle this stale data issue, Microware added "cache care" functions to OS-9, requiring data cache flushing after DMA operations. The initial release of OS-9/68040 did not include support for copyback caching. When copyback support was added in a subsequent release, however, additional caching flexibility was included for the extra options available with the '040. BVM served as a beta test site for Microware's upgraded caching support.

'040 Requires Bus Snooping

For the 68040, bus snooping — a hardware solution to the problem — has to be used to identify access requests to cached data. A request is either sourced or sunk, and the main memory is automatically updated when required. In this case, since the snooping detects the data addresses called from or written to the main memory, the full data cache flushing function is not required and so the OS-9 "cache care" functions have to take this into account.

The other memory issue was the mapping and addressing of the main memory area. A design constraint was that the BVME390 should be a 3U board to address as large a market as possible, as well as include 64M of RAM. This gave rise to a compatibility problem between the 68040, which can happily address up to 4G of memory, organized on an X × 32 bit array, and the constraints imposed by the 24-bit addressing available on the J1 connector of a VMEbus system which gives a maximum addressable memory of 16M. Since OS-9 cannot partition DMA and non-DMA memory areas, the entire 64M of memory needed to be dual ported and snooped.

The hardware design of the BVME390 was heavily influenced by OS-9 operating system requirements. The architecture is 'OS-9 compatible' rather than 'OS-9 unfriendly.'

A page scheme was also extended to allow different types of cache access to the same memory regions. Since the memory is 32 bits wide but the pages are only 24 bits, each location can have two different 4-bit page select codes which allow the same physical memory to appear as non-cached, write-through cached or copyback cached for memory expansion purposes, depending on the page select codes. This

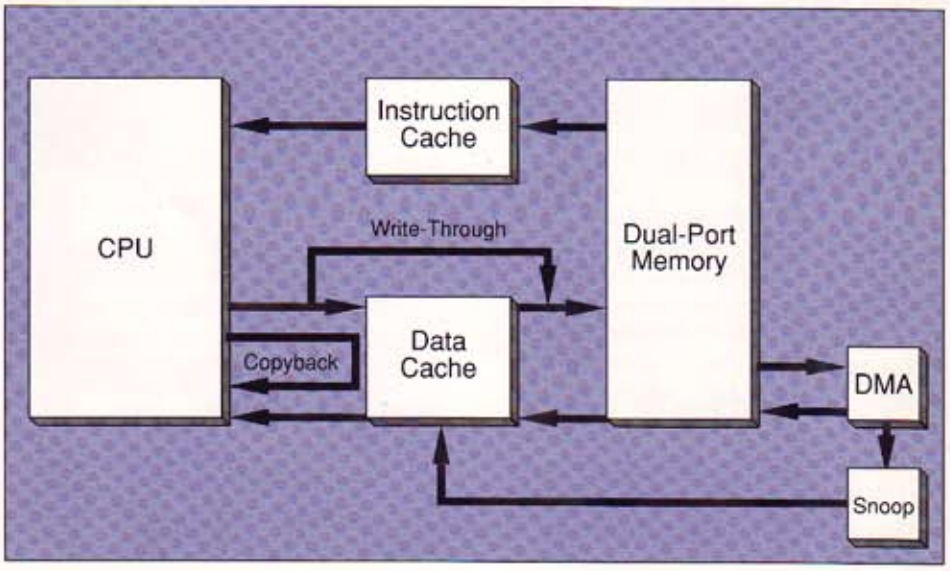
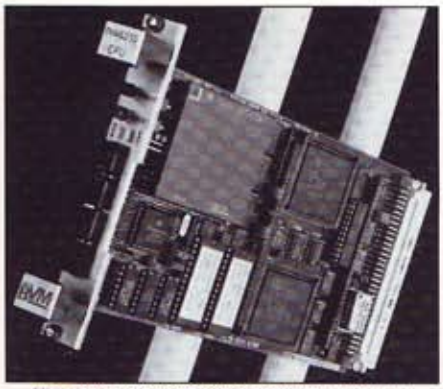


Illustration of OS-9 caching on the BVME390 single board computer. Note: The instruction cache is flushed by the OS-9 Kernel upon *load* and other relevant operations to maintain coherency between caches.



The BVME390 SBC from BVM is designed around a 68040 CPU and optimized for OS-9.

feature is particularly important when, for example, programming or using Flash memory such as the BVME065, where the memory must behave as non-cached during the programming process but then needs to be addressed as write-through cached when in use.

Resolving Other Issues

The original OS-9/68040 distribution did not include control of user memory requests into different caching regions. Three distinct memory regions are typically required:

- copyback for main systems memory
- write-through for non-volatile storage
- no-caching (bus-serialized) for I/O

System State accesses can be controlled by the Transparent Translation Registers (DTT0,1 and ITT0,1), but User State accesses may use the System Security Module (SSM), and therefore the correct setup of the MMU tables is needed. Microware later incorporated the values for the User State caching regions into the initialization module, which, after testing on the BVME390 port, was released as the MVME167 port.

BVM wanted to produce variants of the BVME390 which would run on the three main CPU variants; the 68040, 68EC040 and 68LC040. The 68EC040 was developed by Motorola specifically with low-cost target systems, such as embedded controllers, in mind. It therefore has no MMU or FPU. The 68040 version of the SSM would not run on the cheaper 68EC040 variant, and so BVM wrote a new Access Control Module (ACM) to setup the Transparent Translation Registers for the 68EC040.

At this stage, it was also discovered that the 68EC040 has some slightly different stack frames. Microware was able to modify the OS-9 Kernel and bootstrap code to take account of the new stack frames and the different CPU variants.

The final stage of the porting will be to implement the OS-9 RAMNET interprocess communications package. The BVME390 was designed with a mailbox area and interrupter to handle this with multiple processor boards on the VMEbus. A section of the dual-ported RAM is used for a mailbox data transfer area, which is excluded from the OS-9 search area. The RAMNET implementation will be based on the existing version for the BVME380 68030 CPU. Multiple protocols across the backplane will be possible, enabling OS-9/NET, Internet, NFS, PCLINK and IOF communications concurrently.

Designed for OS-9

It would have been impossible to design in all the various features which allow the user to upgrade transparently to the 68040 without having to modify the system if there had not been a high level of integration between the hardware and the operating system software requirements during the design cycle.

The potential pitfalls are only too real. For example, when Apple introduced the 68040 Quadra range, many existing applications would not migrate to the new machines because of copyback caching problems. A short-term fix was to disable the 68040 caching—hardly an ideal solution!

The hardware design of the BVME390 was heavily influenced by OS-9 operating system requirements. The architecture is "OS-9 compatible" rather than "OS-9 unfriendly" like a 68040 CPU board designed for UNIX. This means that the board is well designed for any OS-9 real-time embedded control application.

Benchmarks against its predecessor, the 68030-based BVME380, at the same clock speed show a 300 to 400 percent improvement in integer performance and a 1000 percent improvement in floating point performance.

David Smith is the technical director at BVM Limited (Southampton, England). BVM specializes in the design, development and manufacture of pluggable boards for VMEbus systems. MSC

New Distributors for Italy, Russia

Nick Rainey, Manager
Microware Systems France

WE ARE PLEASED TO WELCOME TWO NEW DISTRIBUTORS to Microware's worldwide distributor network. Customers in the regions listed below should contact these distributors for Microware's products.

SyAC for Italy

SyAC (System Automation and Control s.r.l.) was founded in 1988 to serve the industrial automation and control markets in Italy. The company is now the authorized distributor of Microware products for Italy.

CALL OR WRITE
Dr. Riccardo Mazzurco
SyAC
Via Ireneo Della Croce, 4
34126 Trieste
Italy
Phone: (39) 40 36 88 81
Fax: (39) 40 36 89 06

The employees at SyAC. Dr. Mazzurco is pictured standing on the right.

RTsoft for Russia, Commonwealth

RTsoft was formed last year to serve the growing real-time products market in the Russian Republic and other members of the Commonwealth of Independent States (formerly the Soviet Union).

CALL OR WRITE
Olga Sinenko
RTsoft
P Box 121 Chernogolovka
Noginskiy District
Moscow Region 142432
Russia
E-Mail: olga@sif.sherna.msk.su
Fax: (7) 095 334 75 00 MSC

OS-9 Data Modules Facilitate Multilingual Message Access

by Robert C. Gaissert
Microware Systems K.K.

CREATING A SOFTWARE PRODUCT FOR DIVERSE LANGUAGE GROUPS ALWAYS presents interesting challenges. Most obvious is that the product must access and display messages in different languages. Developers commonly handle this problem (and perhaps others as well) by compiling different versions of the product, each with messages in a different language. This solution, however, is likely to lead to headaches over source code control, integration and maintenance. It also does not permit the most desirable flexibility of allowing users to choose a language at runtime. Other common solutions to the problem of multilingual message access are to compile in all the messages, thereby sacrificing memory and complicating the source code, or to read them from a file, sacrificing execution speed.

The OS-9 data module facility, widely appreciated for its usefulness in interprocess communication (see, for example, Chuck Wesolowski, "Synchronizing Data Module Access in OS-9," *PIPELINES*, Winter 1992, Vol. 7 No. 1, pp. 16-17), offers an elegant, efficient way to manage multilingual message access. As a software developer, you first design a suitable data structure for the messages. Then, with that structure, you create a different OS-9 data module for each language and load in the appropriate messages.

At runtime, the application simply links to the appropriate module (as specified by, say, an environment variable) and displays whatever messages are contained therein. This solution saves memory, as only one set of messages need be kept in memory at a time, available to multiple processes. As for speed, OS-9 modules are quickly loaded and accessed. When loaded, a data module may "stick" in unneeded memory waiting to link to another process. Finally, the maintenance for multilingual message capability is reduced mostly to updating data modules with new or different application messages.

The basic steps, then, for making such a use of OS-9 data modules are these:

1. Decide on the best data module structure;
2. Write a *load* program to create the data modules and load the application messages into them;
3. Put code in the application so that it may link to the appropriate data module at runtime and access the messages.

Data Module Structure

The best data structure for holding messages will depend on the needs of the application. Significantly, the size of the structure must be known at compile time. The simplest structure would be an array of fixed-length strings:

```
/*****************************************************************/
/*
* msgmod1.h - data structure for OS-9 data module to contain
* application messages
*/

#define COLUMNS  80   /* maximum length of messages expected */
#define ROWS     50   /* maximum number of messages expected */

typedef struct msg_data_t
{
   /* total messages now loaded into module */
   unsigned short total_msgs;
   char msg_a[ROWS][COLUMNS]; /* array containing messages */

} MSG_X;

typedef char MSG_MOD;
/*****************************************************************/
```

In a separate header file, shown below, you would create definitions for the messages for use as an index into the above structure.

```
/*****************************************************************/
/*
* msg.h - definitions of messages
*/

#define FILE_OPEN_ERR 0    /* could not open file */
#define USR_INPUT_ERR 1    /* user input invalid */
```

Robert Gaissert is a senior software engineer at Microware Systems K.K. (Tokyo, Japan). He holds a Ph.D. in English and a Masters degree in business information systems from Georgia State University (Atlanta, Georgia) and a Bachelor of Arts degree in English from West Georgia College (Carollton, Georgia). MSC

New President at Microware's Japanese Subsidiary

MICROWARE RECENTLY APPOINTED KOUJI KANEKO AS PRESIDENT OF MICROware Systems K.K., Microware's wholly-owned subsidiary in Tokyo. Prior to joining Microware K.K., Mr. Kaneko was an executive vice president for Microsoft Company Ltd., the Japanese arm of Microsoft.

Kaneko has an extensive background in both technical development and marketing of technological products. In addition to his position at Microsoft, Kaneko was president and representative director of Nihon Alliant Computer Systems Company, Ltd., senior general manager and director of Nihon Digital Equipment Corporation, and supervisor of the computer systems division of Hitachi Engineering Company, Ltd.

Kaneko brings extensive experience in both computer technology and international business. Under his leadership, Microware K.K. is ready to expand its markets in the coming year. MSC

Our New Staff Members

Tina Cooper recently joined Microware's finance department as a payroll/ fixed assets accountant. Previously, Tina was the controller for Wilson Railway Corporation (Des Moines, Iowa). She holds an Associate of Business degree in computer programming and accounting from the American Institue of Business (Des Moines).

Ray Ellis joined Microware for part-time maintenance. Previously, he worked as a courier for Brenton Banks (Des Moines). Ray is retired from the U.S. Air Force.

Terry Finken-Bayes comes to Microware as the administrative assistant for R&D. Terry holds a Masters of Science degree in counseling from Drake University (Des Moines) and a Bachelor of Science degree in business administration from the University of Iowa (Iowa City).

Troy Frericks is the system administrator for Microware's CD-I Group. Previously, Troy was the system administrator for the State of Iowa Judicial Department (Des Moines).Troy holds a Bachelor of Science degree in computer science from Iowa State University (Ames).

Adam Goldberg joins Microware as a software engineer. Adam recently received his Bachelor of Science degree in computer science from Iowa State University (Ames).

Mark Heilpern comes to Microware as a technical training engineer. Before coming to Microware, Mark was a technical support engineer at Ironics Incorporated (Ithaca, New York).

Denise Landwehr joins Microware as a technical support assistant for Microware's software "Hotline." Prior to joining Microware, Denise was a secretary at Employers Mutual Insurance Company (Des Moines). She holds a clerical diploma from North Iowa Community College (Mason City).

Scott McGee comes to Microware as a software engineer. Scott came to Microware after completing his Bachelor of Science degree in computer science at the University of Utah (Salt Lake City) and working for Whitehall Products (Salt Lake City) as a software engineer.

Renee Merimee is a "Hotline" support engineer at Microware. Renee recently received her Bachelor of Science degree in computer science at Iowa State University (Ames).

Gopal Miglani joins Microware as a senior software engineer. Previously, Gopal was a manager at ICOM Systems (Des Moines) where he developed commercial communications products. Gopal holds a Master of Science degree in computer science from Iowa State University (Ames) and a Bachelor of Engineering degree in electrical engineering from the University of Delhi (Delhi, India).

Uday Naik is a senior software engineer with Microware. Prior to joining Microware, Uday was an associate instructor in computer science at Indiana University (Bloomington). He holds a Master of Science degree in computer science from Indiana University and a Bachelor of Science degree in computer science and engineering from the India Institute of Technology (Bombay, India).

Ann Percy (not pictured) is an office administrator for Microware's British subsidiary. Prior to joining Microware, Ann was a receptionist and clerk with SMH Ltd. (Eastleigh, England).

Boisy Pitre comes to Microware as a associate software engineer. Boisy is the founding president of the OS-9 Users Group and attended the University of Southern Mississippi (Hattiesburg).

Michelle Schwartz is a producer with Microware's CD-I Publishing Group. Before joining Microware, Michelle was the manager of field communications for the Principal Financial Group (Des Moines). Michelle holds a Bachelor of Arts degree in speech and journalism from the University of Northern Iowa (Cedar Falls).

Bret Wilkening comes to Microware as an internal systems administrator. Prior to coming to Microware, Bret headed up the computer department at Royal Office Systems (Des Moines). Bret holds Associate of Arts degrees in environmental control technology from Iowa Central Community College (Fort Dodge) and electronics engineering technology from the National Institute of Technology (West Des Moines). MSC

Continued from Page Three

tinues until the message reaches its final destination, usually a telephone.

This presents two inherent problems. First, signals are converted (A/D and D/A) unnecessarily over long distances. Second, in the case of digital information, the conversion introduces error into the data transmission, resulting in lower transfer speeds and unpredictable error rates.

ISDN addresses both problems by providing a digital carrier from end to end. This allows users to use of reliable protocols, if needed, and to achieve predictable error rates. Analog information is converted only at the endpoints.

Overview of ISDN

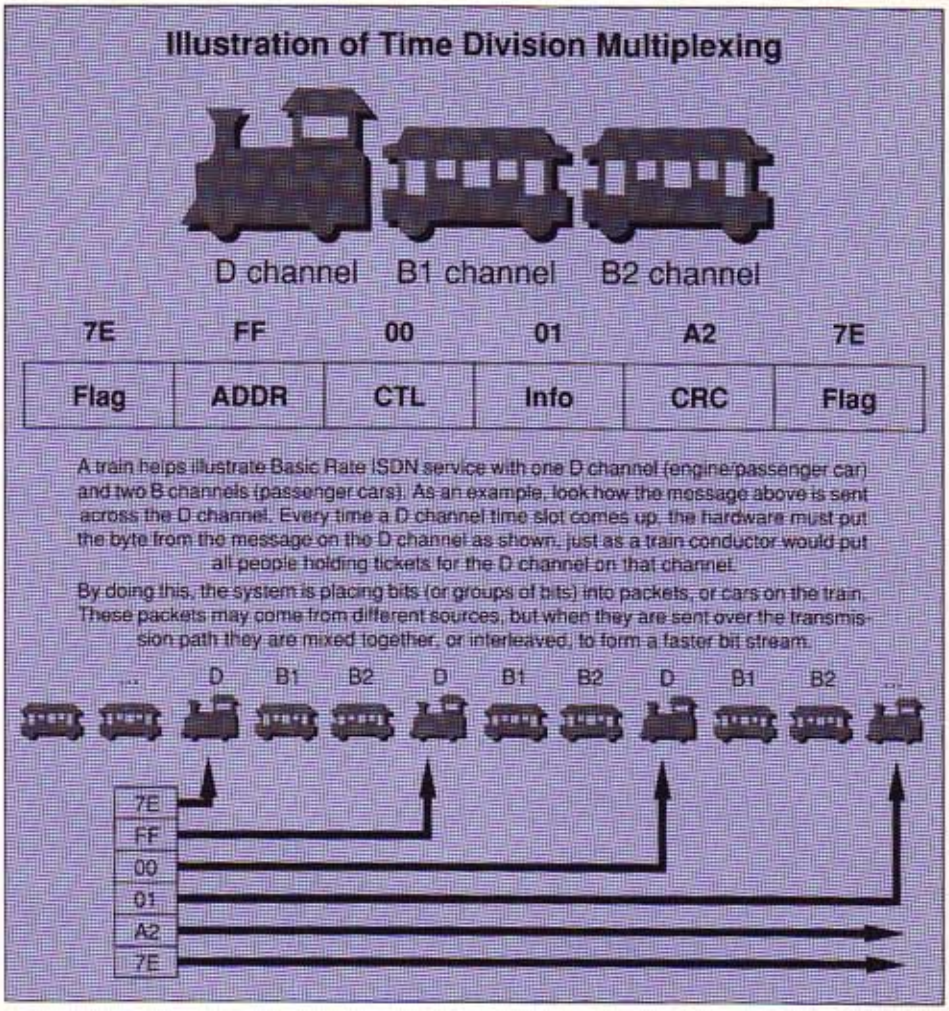
Digital communication systems send multiple signals over a single transmission path. Each transmission path is made up of continuously moving "message frames." This method of sending multiple messages, or data packets, from different sources over a single transmission path is called "time division multiplexing." ISDN uses time division multiplexing at the physical layer to create three separate channels across one physical pair of wires.

Each message frame consists of two types of channels:

- A control channel called the D channel
- Two or more bearer channels, referred to as B channels

A passenger train helps illustrate the function of each channel. In its simplest form, the D channel is like a train engine, while the B channels are like the passenger cars. However, the D channel can also act as a passenger car. For the basic ISDN service, there would be one D channel (engine/passenger car) and two B channels (passenger cars) as shown at the right. When people buy a ticket for the train, they buy a ticket for a particular car, D, B1 or B2. When a train pulls in, people with tickets for B1 get in the first car and people with tickets for B2 get in the second car. When B1 is full, people holding tickets for that car must wait for the next train.

This is the same concept that ISDN uses to send messages across the moving message frames. When you send data (for example, when you make a telephone call), the data waits for a free packet. The data is loaded into the different channels within this packet, and then the packet is routed to its final destination, just like people getting on a train are routed to their destination.



Two Classes of ISDN Service

ISDN is currently divided into two classes: Basic Rate and Primary Rate. Basic Rate ISDN (supported in this release of ISM) provides message frames at 192K/sec. broken into two B channels and a D channel. The 16K/sec. D channel's primary purpose is to control what resources are using the B channels. This is known as "call control." The D channel can also be used to pass data.

The two 64K/sec. B channels are used to pass data. These channels are shared resources that must be requested from the network. The remaining 48 bits of each frame are used for maintenance purposes.

Primary Rate ISDN (not currently supported by ISM) provides message frames at either 1.544M/sec. divided into 23 B channels and a D channel, or the European standard of 2.048M/sec. split into 31 B channels and a D channel.

ISDN File Manager Architecture

The ISDN File Manager, or ISM, package consists of four major functional modules, all of which are compact, ROMable and easily integrated into OS-9 or OS-9000 system configurations.

ISDN File Manager

The ISDN File Manager is a hardware-independent, re-entrant subroutine package that provides a programming interface to the ISDN network and manages the call control, data transmission and error detection/correction functions. ISM adheres to the OSI network model and implements the CCITT Q.921 Data Link and Q.931 Call Control functions.

Configuration Modules

Configuration modules are called by ISM to handle portions of the call control functions when communicating with digital switching systems. As call control protocols are not fully compatible across digital switching systems, this permits ISM to be

easily reconfigured to work with various manufacturer's switches.

Current configuration modules support the AT&T 5ESS /5E6 and NTT (INS Net64) switches. Microware will provide assistance to ISM licensors to produce new configuration modules for alternative switch systems.

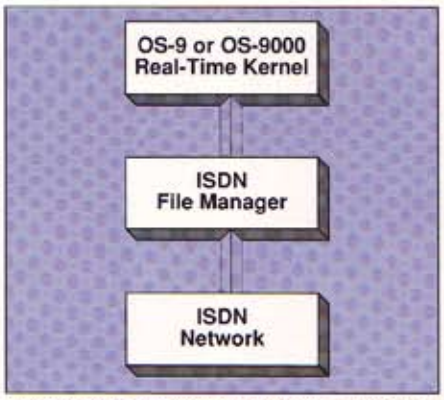
Protocol Modules

Protocol modules are called by ISM to implement the specific type of protocol used for communicating across an ISDN B channel. The ISM package includes three protocol modules: ***NULL*** for voice calls only, ***RAW*** for transparent data transfers and ***LAP-B*** for reliable data transfers. ISM also allows dynamic runtime switching of the protocol modules used by an application.

Device Drivers and Descriptors

ISM device drivers are hardware-dependent, interrupt-driven service routines that manipulate the physical network hardware to transmit and receive packets. Device descriptors are table entry modules that specify operating parameters for an ISDN network path, such as which configuration and protocol modules will be used for the connection.

The ISM package contains device driver and descriptor source code for the AMD 79C30 and Siemens 82525 HDLC communication controllers. These sources can be used as-is for similar hardware designs, or as a reference when creating device drivers for other communication controllers.



How the ISDN File Manager (ISM) works with the OS-9 and OS-9000 kernels.

Simplified Network Access

The CCITT Q.931 standard specifies over 30 primitive functions for D channel call control. To simplify call control programming, the ISM package includes a library called ***isdnlib.l***. This library of condensed, high-level functions (such as ***dialup()***) reduces the need to call Q.931 primitives directly, simplifying application development.

Hardware Design Included

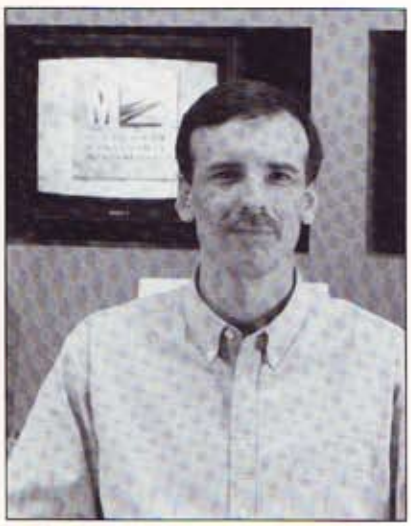
During development of the ISM package, Microware designed and built a Basic Rate ISDN interface card called the **Terminal Adaptor Microware Interface (TAMI)**. This low-cost board can be easily incorporated into new designs to produce a drop-in Basic Rate ISDN hardware/software solution. Microware will provide the schematics of the board to any ISM licensee upon request.

Until now, networking companies have provided products that, in most cases, are difficult to integrate into computer environments. Microware's unique, leading-edge concepts allow networking services to grow out of the operating systems themselves. This allows Microware's products to include more transparent interfaces to networking services.

Curt Schwaderer is an ISDN development engineer in Microware's wide area networks group. Before joining Microware, Curt was with Electrospace Systems (Richardson, Texas), a company that develops secure telecommunications switching systems. MSC

CD-I Two in Review

by Jeff Ames
Microware Systems Corporation



REPRESENTATIVES FROM MICROWARE'S U.S., British and Japanese operations recently travelled to Los Angeles, California, to participate in *CD-I Two International, the Second Annual Publishing and Developers' Conference and Exposition*. The three-day event, sponsored by Philips Consumer Electronics, Matsushita Electric Industrial Company and Sony Corporation, was designed to keep publishers, producers and program developers abreast of the latest developments in CD-I. Microware has played a key role in the design and development of CD-I since its inception. Microware's Compact Disc Real-Time Operating System (CD-RTOS) is the operating system found in every CD-I player worldwide.

Microware's presence at the conference was notable. On the exhibit floor, visitors to the Microware booth were able to view some of Microware's latest CD-I discs, including: *CD-I Reversi*, a new consumer game due for release early next year; *A Tour Of The Grand Canyon*, produced in cooperation with Reader's Digest; and *Max The Dragon's Adventures In Outer Space*, a new children's program produced jointly by Microware and Meredith Corporation. Eric Miller, Microware's director of multimedia, provided technical insights into Full-Motion Video (FMV), both on the exhibit floor and at a roundtable panel discussion. Chuck Spong, president and CEO of MicroMall, Inc., a Microware subsidiary, demonstrated the uses of CD-I technology in the field of electronic merchandising.

In addition to the Microware booth, Microware-produced CD-I discs were evident throughout the exhibit hall. Gold-Star Company Ltd. of Korea used a demonstration disc produced at Microware's Des Moines CD-I studio to help officially introduce their new CD-I consumer player, due on the market next year. And Sony Corporation, displaying the world's first portable CD-I player, showed *Being A Marketing Organization*, a disc produced by Microware in cooperation with The Principal Financial Group.

Jeff Ames is the manager of Microware's Des Moines CD-I studio. MSC

ON THE C SIDE

Trap Handlers in C for OS-9

by Ric Yeates
Microware Systems Corporation

TRAP HANDLERS PROVIDE AN EXCELLENT MEANS TO IMPLEMENT SHARED LIBRARies. With trap handlers many applications can share the same code even though each one is a separate module. This provides for smaller modules, thus more efficient use of memory. You do pay a price though; each call to the trap handler has significantly more overhead than simply ***bsr***–ing to a routine.

Before examining the accompanying sample code, read Chapter 5 of the *OS-9 Technical Manual*. This will introduce you to the basic concepts of trap handlers. The trap handler presented here has several advantages over the one in the technical manual:

- Dispatch table drive
- Subroutines written in C
- Support for parameter passing and return values
- Automatic update of ***_environ*** and ***errno***

The main dilemma when dealing with trap handlers is the code contained within the trap handler executes with a different global data pointer than the calling module. This can cause problems related to ***_environ*** and ***errno***. This is handled by passing the address of these two variables to the trap handler initialization routine. Then, each time a function in the trap handler is called, the necessary values are read. Each time a trap handler function exits, we update ***errno*** and ***_environ*** in case the called function modified them.

Three files make up this example. These files contain constructs that are specific to Ultra C, Microware's new ANSI C compiler:

- tstart.a—the trap handler entry points and dispatch code for the C routines
- ctrap.c—the C routines and the dispatch table
- traptst.c—a C program to test the trap handler

To compile the three files into the trap handler and test program, use the following command lines:

1. r68 tstart.a -o=tstart.r
2. cc -r ctrap.c -eas
3. cc -k tstart.r ctrap.r -l=/h0/LIB/os_lib.l -l=/h0/LIB/sys.l -f=ctrap
4. cc traptst.c

Then run ***traptst***. If all is right, it should print some mathematical truths.

```
tstart.a
--------
        use  <oskdefs.d>

AttrRevs set (ReEnt)<<8 (sharable)
TypeLang set (TrapLib<<8)+Objct

        psect traphand,TypeLang,AttrRevs,0,0,TrapEnt
        dc.l TrapInit
        dc.l TrapTerm

                vsect
User_Ret_PC     ds.l 1    return address
Func_Code       ds.w 1    function call
User_a6         ds.l 1    caller's a6
errno_ptr       ds.l 1    pointer to caller's errno
errno:          ds.l 1    trap handler's errno
 environ_ptr    ds.l 1    pointer to caller's  environ
_environ:       ds.l 1    trap handler's  _environ
                ends


*******************************
* Subroutine TrapInit
* User Trap initialization entry point
*
* Passed: d0.w = vector #
*         d1.l = (optional) additional static storage
*         d2-d7 = caller's registers
*         (a0) = trap handler module name
*         (a1) = trap handler execution entry point (TrapEnt)
*         (a2)  trap module pointer
*         (a3) = user's errno variable
*         (a4) = user's  environ variable
*         (a6) = trap handler static storage pointer
*         (a7)  trap entry stack frame pointer
*
*
* The stack looks like this:
*                 .-------------------------.
*          +8     | caller's return PC      |
*                 |-------------+-----------|
*          +4     | func code   | vector #  |
*                 |-------------+-----------|
*        (a7)->   | caller's (a6) register  |
*                 '-------------------------'

TrapInit: move.l a3,errno_ptr(a6)  save pointer to user's errno
          move.l a4,_environ_ptr(a6) save ptr to user's  environ
          move.l (sp)+,a6           restore user's a6 pointer
          addq.l #4,sp              skip function code and vector
          rts

*******************************
* Subroutine TrapEnt
* User Trap entry point
*
* Passed: d0-d7 = caller's registers
*         a0-a5 = caller's registers
*         (a6) = trap handler static storage pointer
*         (a7)  trap entry stack frame pointer
*
* Returns: d0 = -1 for an error, else function specific value
*
* The stack looks like this:
*                 .-------------------------.
*                 |    caller's stacked     |
*          +16    |      parameters         |
*                 |-------------------------|
*          +12    |     trap return PC      |
*                 |-------------------------|
*          +8     |    caller's return PC   |
*                 |-------------+-----------|
*          +4     | func code   | vector #  |
*                 |-------------+-----------|
*        (a7)->   | caller's (a6) register  |
*                 '-------------------------'
```

Continued

```
TrapEnt:move.l (sp)+,User_a6(a6)    save user's a6
        move.w (sp)+,Func_Code(a6)  save function code
        adda.l #6,sp                skip vector # and trap ret PC
        move.l (sp)+,User_Ret_PC(a6) save return PC
        pea.l Func_Ret(pc)          install new return address
* at this point the stack and registers are in the standard
* C calling convention format.
        move.l #0,-(sp)             room for function address
        movem.l d0/a0,-(sp)         save registers
stacked set 4*2
        move.w Func_Code(a6),d0     get desired function code
        ext.l d0                    make into long
        cmpi.l #NUM_SUBS,d0         check range
        bhs.s Err_Exit              too high...
        asl.l #2,d0                 multiply by 4
        lea disp_table(a6),a0       get base of table
        movea.l (a0,d0.l),a0        get entry
        move.l a0,stacked(sp)       place before saved registers
        move.l _environ_ptr(a6),a0  get ptr to user's _environ
        move.l (a0),_environ(a6)    install into my _environ
        movem.l (sp)+,d0/a0         pop saved registers
        move.l #0,errno(a6)         clear our errno
        rts                         call routine
Func_Ret move.l User_Ret_PC(a6),-(sp) restore proper return addr
        move.l a0,-(sp)
        tst.l errno(a6)             errno get set?
        beq.s Skip_Errno            no, skip setting user's version
        move.l errno_ptr(a6),a0     get pointer to user's errno
        move.l errno(a6),(a0)       fill in from our version
Skip_Errno move.l _environ_ptr(a6),a0 get ptr to user's  environ
        move.l _environ(a6),(a0)    fill in from our version
        move.l (sp)+,a0
        movea.l User_a6(a6),a6      restore user's a6
        rts                         return to caller

Err_Exit movem.l (sp)+,d0/a0        pop registers
        move.l #0x01ff,errno(a6)    return error #001:255
        adda.l #8,sp                fix stack
        move.l #-1,d0               return -1
        bra.s Func_Ret

TrapTerm: rts

      ends
```

```
ctrap.c
-------
extern int errno;
extern void * environ;

int sub_0(), sub_1(), sub_2(), sub_3();

/*
   Dispatch table is used by tstart.a to determine what
   funtion to call for each function code.
*/
int (*disp_table[])() = {
   sub_0, sub_1, sub_2, sub_3
};

/*
   The following equate is referenced by tstart.a to determine
   the range of valid trap calls. Valid trap calls will range
   from 0 to NUM_SUBS-1
*/
_asm("NUM_SUBS: equ %0", sizeof(disp_table) / sizeof(int (*)()));

int sub_0(int a, int b, int c)
{
   return ((a + b) / c);
}

int sub_1(int a, int b)
{
   return(a + b);
}

int sub_2(int a, int b, int c)
{
```

Continued

```
   return(a / b / c);
}

int sub_3()
{
   /* test filling of errno and _environ */
   errno = 0x11223344;
    environ = (void *)0xffeeddcc;
}
```

```
traptst.c
---------
#include <stdio.h>
#include <errno.h>
#include <string.h>

extern void *_environ;

#define TRAP_VECTOR 6

int tlink(int, char *);

_asm("sub_0: tcall %0,0", TRAP_VECTOR);
_asm("sub_1: tcall %0,1", TRAP_VECTOR);
_asm("sub_2: tcall %0,2", TRAP_VECTOR);
_asm("sub_3: tcall %0,3", TRAP_VECTOR);
_asm("sub_4: tcall %0,4", TRAP_VECTOR);

main()
{
 int a;

   if (tlink(TRAP_VECTOR, "ctrap") == -1) {
      fprintf(stderr,
          "can't F$TLink to 'ctrap' - %s\n",
          strerror(errno));
      exit(errno);
   }
   printf("8 + 12 = %d\n", sub_1(8, 12));
   printf("(5 + 3) / 4 = %d\n", sub_0(5, 3, 4));
   a = sub_2(1000, 25, 4);
   printf("1000 / 25 / 4 = %d\n", a);
   sub_3();
   if (errno != 0x11223344 || _environ != (void *)0xffeeddcc)
     printf("errno and/or _environ not being passed correctly\n");
   a = sub_4();
   printf("call to 5th function = %d (%s)\n", a, strerror(errno));
}

/* binding for tlink */
/*************************************************************/
/* tlink(trapnum, trapname) link to trap handler */
/* int trapnum;          user trap number (1-15) */
/* char *trapname;       name of trap module (NULL to unlink) */
_asm("tlink: link     a5,#0");
_asm("       movem.l  a0-a2,-(a7)  save regs");
_asm("       movea.l  d1,a0        copy ptr to trap handler name");
_asm("       moveq    #0,d1        no memory override");
_asm("       lea.l errno(a6),a3    pass address of errno");
_asm("       lea.l  _environ(a6),a4pass address of _environ");
_asm("       OS9      F$TLink      link to trap handler");
_asm("       bcc.s    tlink99      exit if no error");
_asm("       move.l d1,errno(a6)   save error number for caller");
_asm("       moveq    #-1,d0       return error status");
_asm("tlink99 movem.l (a7)+,a0-a2 restore regs");
_asm("       unlk     a5");
_asm("       rts");
```

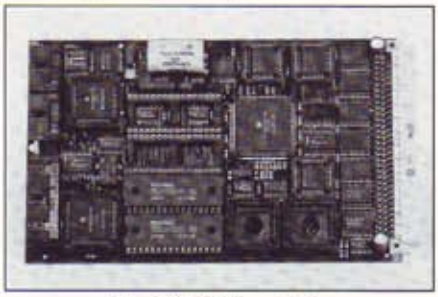
Ric Yeates is a principal software engineer at Microware. During his five years at Microware, Ric has been on the Ultra C ANSI C compiler and OS-9000 development teams, and was previously a training and education instructor. MSC

New Vendor Products

IF YOU HAVE NEW HARDWARE OR SOFTWARE PRODucts that run under OS-9 or OS-9000, please submit a press release and black & white photograph of the product for consideration for publication in *PIPELINES*. All materials should be sent to the Editor of *PIPELINES* at the address on page 2. For more information, call Steve Simpson at (515) 224-1929.

'330, '340 SBCs from Actis

Actis Computer S.A. (Geneva, Switzerland) recently introduced two new single board computers. Their 3U **SBC-330** is based on a 16.8 MHz 68330 CPU and features up to 1.25M battery-backed SRAM, up to 3M EPROM and two RS-232 ports. The board features CMOS components for reduced power consumption.



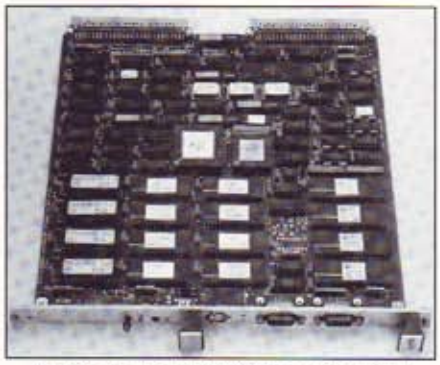
The SBC-330 from Actis.

The 3U **SBC-340** is based on a 16 MHz 68340 CPU. A two-channel DMA controller, two serial port and a double 16-bit timer are featured on the 68340. In addition, the SBC-340 features 4M DRAM, a battery-backed real-time clock and calendar, flexible disk controller and a SCSI bus controller. The all-CMOS design keeps power consumption low.

CALL OR WRITE
Actis Computer S.A.
16 chemin de Aulx
Plan-les-Ouates
CH-122B Geneva
Switzerland
Phone: (41) 22 794 43 35
Fax: (41) 22 794 43 91

Mil-Spec SBC from Alphi Technology

Alphi Technology Corporation (Tempe, Arizona) recently announced the release of their 100 percent CMOS **CPUC32** single board computer. The 6U VMEbus board is built around a 68030 and features ruggedized mil-spec construction and military-qualified documentation. Onboard, the CPUC32 includes up to 4M battery-backed zero wait-state SRAM, eight serial ports and two parallel ports.



Alphi Technology's 68030-based CPUC32.

CALL OR WRITE
Alain Brunet
Alphi Technology Corporation
6202 South Maple Avenue #128
Tempe, Arizona 85283
Phone: (602) 838-2428
Fax: (602) 838-4477

Open Architecture Bus from Arcom

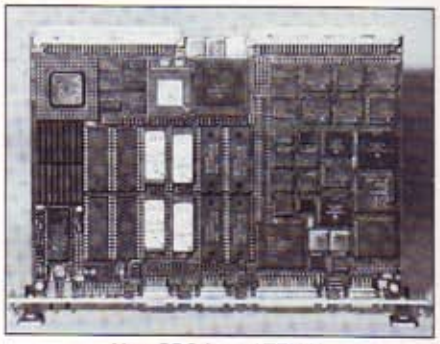
Arcom Control Systems Ltd. (Cambridge, England) has announced the release of their **SCIM** open architecture bus. SCIM, for Standard Computer Interface Module, accommodates up to 16 data and 24 address lines, four interrupts, plus DMA channels and serial lines. Ready-to-use modules are available from Arcom for VMEbus, STEbus and PCbus host carrier boards. SCIM modules measure 120 mm × 50 mm.

Arcom's *Catalogue 5* includes extensive information about Arcom's line of VMEbus and STEbus systems. *Catalogue 5* is available free from Arcom.

CALL OR WRITE
Paul Cuthbert
Arcom Control Systems Ltd.
Units 8-10, Clifton Road
Cambridge CB1 4WH
England
Phone: (44) 223 411200
Fax: (44) 223 410457

'030 SBC, Serial Board from ATENIX

ATENIX s.r.l. (Verona, Italy) recently announced the release of two new products. The **ATX-630** is a 6U VMEbus single board computer based on either a 25 or 40 MHz 68030 or 68EC030 CPU. The SBC features optional 68881/2 FPCP, up to 2M battery-backed zero wait-state private SRAM, up to 2M battery-backed dual-ported RAM, up to 8M dual-ported DRAM, up to 2M EPROM, optional LANCE Ethernet controller, optional SCSI controller, flexible disk controller, DMA controller, battery-backed real-time clock, two RS-232 channels, one Centronics port and watchdog timer.



New SBC from ATENIX.

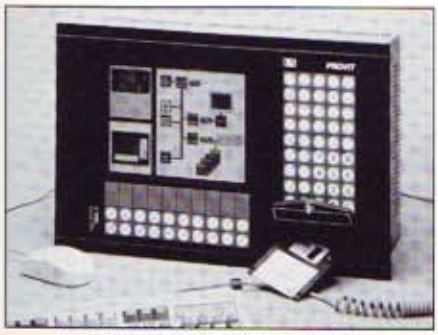
The **ATX-250** is an optoinsulated intelligent serial board based on a 25 or 40 MHz 68EC030 with 12 configurable (RS-232/422/485) serial channels. The board also includes up to 128K private zero wait-state SRAM, up to 256K dual-ported SRAM, up to 256K EPROM and six 16-bit programmable timers.

CALL OR WRITE
Marco Montresor
ATENIX s.r.l
via F.lli Morandini 4/2
37136 Verona
Italy
Phone/Fax: (39) 45 8201760

OS-9 Workstation from B&R

B&R Industrial Automation Corporation (Roswell, Georgia) recently released their **PROVIT 1800** workstation. The PROVIT 1800 runs OS-9 on a 25 MHz 68020 CPU with FPCP and features a 68000 graphics CPU, 68000 communications CPU, up to 8M DRAM, up to 2M EPROM or Flash EPROM, 1.44M 3½ inch flexible disk drive, 52M hard disk drive, four serial ports, keyboard port, RGB monitor port and ARCNET networking interface. The workstation is contained in a standard 19-inch rack mount and includes an 11-inch 640 × 480 thin-film-transistor (TFT) display, 12

numeric keys, 20 software-definable function "soft" keys and 33 function keys.



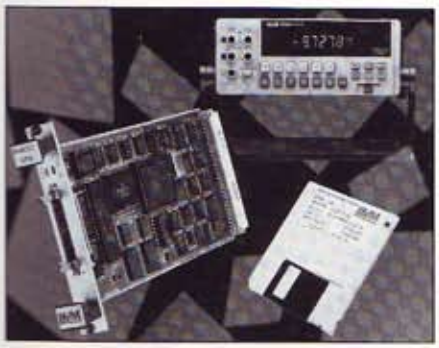
The PROVIT 1800 OS-9 workstation.

B&R's **SPECTO-S** process graphics software is also available for the PROVIT 1800. The SPECTO-S editor can be used to develop static process, machine, information and alarm displays. The editor also sets up variable fields, configures the "soft" keys and defines the operation of the function keys. Screens are then displayed with real-time data using the run-time portion of SPECTO-S.

CALL OR WRITE
Carl Hamilton
B&R Industrial Automation Corporation
1325 Northmeadow Parkway S-130
Roswell, Georgia 30076
Phone: (404) 772-0400
Fax: (404) 772-0243

GPIB Board, More from BVM

Two new boards and an upgraded software package were recently announced by BVM Limited (Southampton, England). The **BVME227** is a 3U VMEbus GPIB interface for instrumentation communications under the IEEE 488.2 protocol. Based on the TMS9914A GPIB controller chip, the BVME227 can achieve data transfer rates of 500K/sec. Managed by an MC68440 controller, true double-buffering allows concurrent access to the on-board 256K RAM from both the GPIB interface and the VMEbus without arbitration.



BVM's GPIB interface for the VMEbus.

The **BVME681** pluggable disk module includes a high-performance VMEbus BVME130 disk controller, dual-ported RAM, on-board DMA controller, a 4M 3½ inch flexible disk drive and up to 200M Winchester disk drive. The BVME681 is available in both 3U and 6U formats.

PCLINK Version 2 software package allows data transfers from PCs to OS-9 systems. The latest version adds support for Windows 3.x via a 10M/sec. Ethernet connection.

CALL OR WRITE
Rod Clarke
Managing Director
BVM Limited
Flanders Road, Hedge End
Southampton, Hampshire SO3 3LG
England
Phone: (44) 703 270770
Fax: (44) 489 783589

VMEbus-to-AS/400 Connection from Compcontrol

Compcontrol Inc. (Los Gatos, California) announced the release of their **CC140** TokenRing LAN adapter for VMEbus systems. The CC140 supports OS-9's TCP/IP protocol and includes remote login and file transfer facilities. The board supports both 4 and 16M/sec. transfer, and is compatible with the IEEE 802.5 and ISO 8802/5 standards.

CALL OR WRITE
Rod Johnson
Compcontrol Inc.
15466 Los Gatos Boulevard, Suite 109-365
Los Gatos, California 95032
Phone: (408) 356-3817
Fax: (408) 356-1755

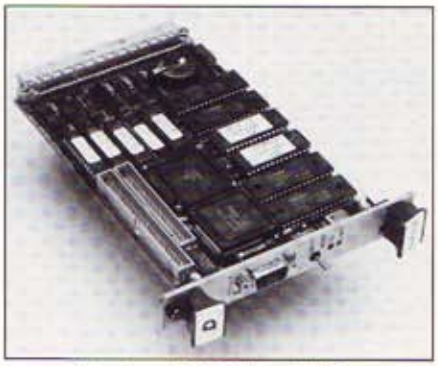
Data Manager from Delmar

DataDex is a free-form data management package from Delmar Company (Middletown, Delaware). DataDex keeps records in a manner similar to a Rolodex card file with titled "cards" that are used to index information. The package features on-line help, variable record size and interactive installation utility.

CALL OR WRITE
Delmar Company
PO Box 78
Middletown, Delaware 19709
Phone: (302) 378-2555
Fax: (302) 378-2556

Dynatem's New '332 SBC

Dynatem Inc. (Irvine, California) recently announced the release of a new 68332-based SBC. The **DCPU332** is a 3U VMEbus single board computer built around a 16.67 MHz 68332 CPU. In addition to the features of the 68332, the DCPU332 features up to 2M battery-backed dual-ported SRAM, up to 512K EPROM, 53C400 SCSI controller, battery-backed real-time clock/calendar and mailbox interrupts.



Dynatem's 68332-based SBC.

CALL OR WRITE
Dynatem Inc.
15795 Rockfield Boulevard, Suite G
Irvine, California 92718
Phone: (714) 855-3235
Fax: (714) 770-3481

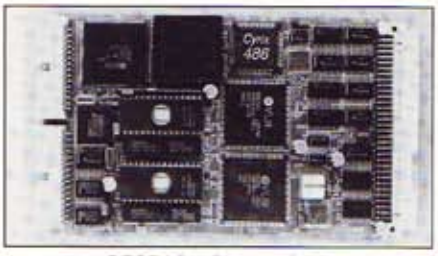
New Publication for OS-9 Users

Fat Cat Publications (Toluca Lake, California) recently began publishing the OS-9 *Underground* newsletter. The publication includes articles on the MM/1, CoCo, TC-70 and Sys IV systems.

CALL OR WRITE
Alan Sheltra, Editor
The OS-9 Underground
Fat Cat Publications
4650 Cahuenga Boulevard, Suite 7
Toluca Lake, California 91602
Phone: (818) 761-4135

New Products from GESPAC

New products from GESPAC, Inc. (Mesa, Arizona) include two SBCs, a 32-bit graphics controller, a memory card drive and Japanese support for their windowing product. The **GESMPU-46** is a 3U G-64/96 bus single board computer built around a 20 MHz Cyrix 486 CPU and features 4M or 8M DRAM, two serial ports (COM1 and COM2), a bidirectional parallel printer port (LPT1), a flexible disk controller and an IDE hard disk interface.



GESPAC's G-64/96 SBC.

The **MPL-4082** is a 3U G-64 bus, full-CMOS SBC built around a 16 or 25 MHz 68EC020. The board consumes 300 mA at 5V and features up to 4M battery-backed

RAM and EPROM, two RS-232 ports, 40 TTL I/O lines, five 16-bit timers, a real-time clock/calendar, and a powerfail detection and watchdog circuit.

The **GESVIG-24** is a 6U VMEbus graphics controller designed around a 20 MHz Hitachi Graphics Drawing Processor (GDP). The board can display color images with a resolution up to 1280 × 1024 pixels on a 110 MHz monitor, or 1024 × 780 pixels on a 64 MHz VGA-type monitor. Video memory is simultaneously accessible from the GDP chip or from the VMEbus in a full 32-bit wide bitmap configuration.

The **MCRW-B** open frame Memory Card Drive is compatible with all types of JEIDA 4.0 and PCMCIA memory cards. The drive features a built-in RS-232 interface and a set of commands for read/write operations. The MCRW-B has the form factor of a standard 3½ inch disk drive.

GESPAC has upgraded their **G-Windows** GUI to support the more-than-500 Katakana, Hiragana and Kanji characters for Japanese writing. The characters are coded using the standard JIS and Shift JIS codes.

For a free 68-page product catalog of GESPAC's products, call or write at the location below.

CALL OR WRITE
Cosma Pabouctsidis
GESPAC, Inc.
500 West Hoover Avenue
Mesa, Arizona 85210
Phone: (602) 962-5559
Fax: (602) 962-5750

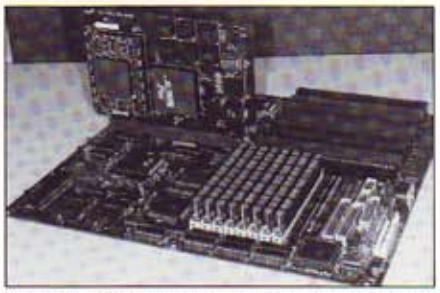
FlexeLint 5.0 Available from Gimpel

Version 5.0 of **FlexeLint** is now available from Gimpel Software (Collegeville, Pennsylvania). The new version of this C source code analysis tool features POSIX and ANSI conformance checking. Non-POSIX and non-ANSI features and functions in C code will be flagged when processed through FlexeLint.

CALL OR WRITE
Anneliese Gimpel
Gimpel Software
3207 Hogarth Lane
Collegeville, Pennsylvania 19426
Phone: (215) 584-4261
Fax: (215) 584-4266

EISA Bus Motherboard from GMX

GMX Inc. (Northbrook, Illinois) recently introduced their **ESA-MB** with interchangeable CPU modules. The ESA-MB EISA bus motherboard fits into the EISA bus and allows a variety of CPU types to be connected to the EISA bus. The ESA-MB is designed around Intel's 82350DT EISA chip set and features up to 256M of high-speed DRAM, 8K battery-backed RAM, eight expansion slots, IDE hard disk interface, flexible disk controller, two RS-232 ports, an 8-bit bidirectional parallel port, AT-style keyboard interface, battery-backed clock and watchdog. CPU modules include a 33 MHz 80486 DX, 40 MHz 68EC030 and 25 MHz 68040/68LC040.



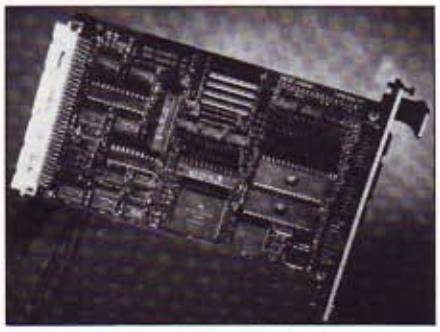
The ESA-MB provides for interchangeable CPUs.

GMX also announced the release of their **ISA-8S** and **ISA-8S9** serial interfaces for ISA or EISA bus systems. The ISA-8S includes eight 6-pin telephone-type connectors that are accessible from the back panel. The ISA-8S9 has two 40-pin header connectors which can be cabled to remotely-mounted DB-9 or other type connectors.

CALL OR WRITE
GMX Inc.
3223 Arnold Lane
Northbrook, Illinois 60062
Phone: (708) 559-0909
Fax: (708) 559-0942

Low-Cost VMEbus SBC from GreenSpring

The 3U VMEbus **SBC1-E** from GreenSpring Computers (Menlo Park, California) is based on a CMOS 16 MHz 68HC000 CPU and features up to 2M zero wait-state DRAM, up to 896K EPROM or Flash EPROM, two serial ports, 16-bit counter/timer and battery-backed real-time clock.

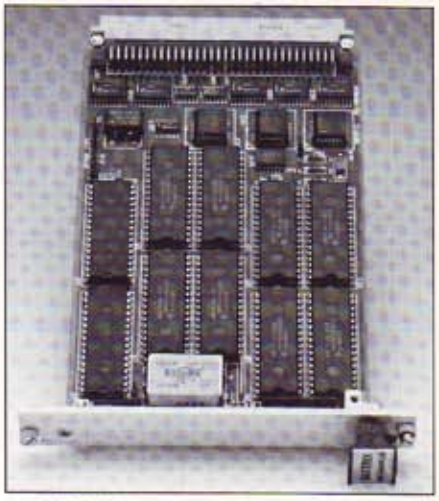


GreenSpring's SBC1-E.

CALL OR WRITE
Kim Rubin
GreenSpring Computers
1204 O'Brien Drive
Menlo Park, California 94025
Phone: (415) 327-1200

Memory Board, Enclosure from MATRIX

MATRIX Corporation (Raleigh, North Carolina) recently introduced a new memory board and a rugged system enclosure. Their **RAMROM** memory board is a 3U VMEbus board that includes up to 4M battery-backed SRAM and two Flash EPROM sockets. RAMROM is addressable as a 24-bit address slave, and supports both 8- and 16-bit data transfers. The board is available in two versions: MSX-RAMROM is suitable for harsh environments where continuous operation from –40° to +85°C is required. The MS-RAMROM operates from 0° to +70°C.



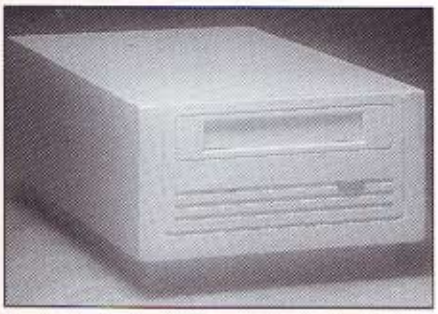
RAMROM memory board from MATRIX.

The **ENC50** is a shock- and vibration-isolated VMEbus enclosure that is designed for weight-sensitive vehicular, airborne and shipboard applications. The ENC50 supports up to a 15-slot backplane, power supply, fans and hard drives in an isolated subchassis. Six low-frequency mounts are used to provide shock and vibration isolation in the three principal axes. Additional protection for disk storage devices is provided by secondary shock and vibration isolation of the disk drive tray.

CALL OR WRITE
MATRIX Corporation
1203 New Hope Road
Raleigh, North Carolina 27610
Phone: (919) 231-8000
Fax: (919) 231-8001

Mass Storage Subsystems from Maynard

Maynard Electronics, Inc. (Lake Mary, Florida) recently announced the release of and OS-9 support for two new mass storage subsystems. The **Anaconda 1350** is a 1.35G SCSI-based tape drive that supports transfer rates of 36M/minute. The Anaconda 1350 is backward compatible with other Maynard Viper series tape drives.



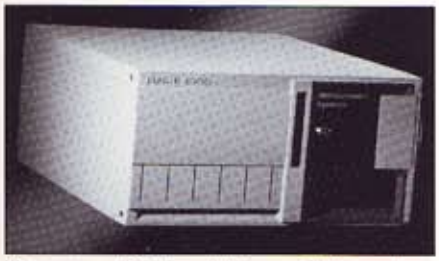
The Python DAT drive from Maynard.

The **Python** family of SCSI-based digital audio tape (DAT) drives provides storage of up to 8G on a single tape. Python drives are available in either standard or DDS-DC (Digital Data Storage Data Compression) data compression versions.

CALL OR WRITE

Maynard Electronics, Inc.
36 Skyline Drive
Lake Mary, Florida 32746
Phone: 1-800-821-8782 (U.S. Only)
or (407) 263-3500
Fax: (407) 263-3555

Data Acquisition System from Measurement Systems



Measurement Systems' data acquisition system.

The **Magus 4000** Data Acquisition System from Measurement Systems (Newbury, England) features either a 33 MHz 486 CPU or 66 MHz DX2 486 CPU with turbo cache, both on the EISA bus. The system is fitted with a 1.4M 3½ inch flexible drive and a 200M Winchester drive, up to 256M RAM, 7-channel DMA controller, two RS-232 ports, one parallel port, Ethernet and TCP/IP interface and software, and backplane data transfers up to 33M/sec.

CALL OR WRITE

Measurement Systems
Units 4B/7B, Faraday Road
Newbury, Berkshire RG13 2AD
England
Phone: (44) 635 42677
Fax: (44) 635 31023

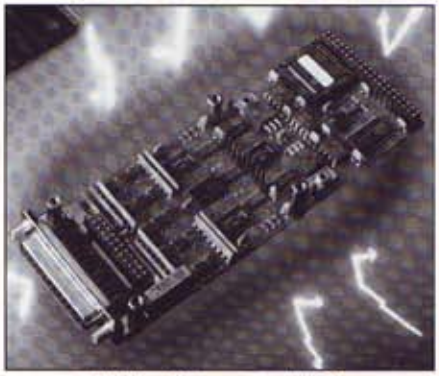
New M-Modules, Boards from MEN

MEN Mikro Elektronik GmbH (Nürnberg, Germany) recently announced the release of two new VMEbus **M-Module** Standard I/O base boards and two new M-Modules. These products comply with electromagnetic compatibility (EMC) and electrostatic discharge (ESD) provisions of the IEC 801 standard.

The 3U VMEbus **B201** and **B202** M-Module base boards each have an A24/D16 interface, and provide one and two M-Module slots respectively.

The **M22** M-Module has eight ESD-protected transistor outputs and switches a load of 2A per channel. The isolation voltage of the M22 is 2kV with a leakage distance of 6 mm.

The **M24** has 16 ESD-protected binary inputs with nominal input voltage of 12-36 volts with a typical input current of 5mA.



MEN's ESD-protected M24.

CALL OR WRITE

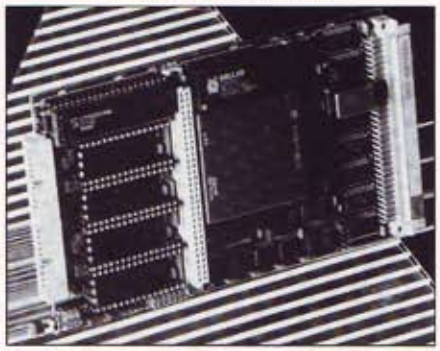
MEN Mikro Elektronik GmbH
Wiesentalstraße 40
W-8500 Nürnberg 90
Germany
Phone: (49) 911/99 33 5-0
Fax: (49) 911/99 33 5-99

G-96 68040 SBC from MII

MII (Puiseux-Pontoise, France) recently released their **GMI-CPU12** single board computer for the G-96 bus. The board features a 25 or 33 MHz 68040 CPU, 4M DRAM, up to 2M EPROM, two serial ports, real-time clock and watchdog.

CALL OR WRITE

J-P Potez
MII
2, Grande rue
95650 Puiseux-Pontoise
France
Phone: (33) 1.34.46.12.25
Fax: (33) 1.34.46.13.72



The 68040-based GMI-CPU12 from MII.

Long List of New Products from Mizar

Mizar, Inc. (Carrollton, Texas) recently announced the release of more than 20 new products. Mizar's **multiprocessor support for OS-9** is a loosely-coupled implementation that uses TCP/IP across a VMEbus backplane. As many as 21 CPUs can be coupled in the system. In Mizar's global memory model, each CPU has dual-ported memory that is accessible by every other CPU in the system. Their shared memory pool model defines one common memory pool on the VMEbus that is accessible by all CPUs.

The following products were announced at BUSCON/East by Mizar:

- **MZ 7142** Dual 68040 SBC – Two 68040 CPUs, up to 32M RAM, up to 1M EPROM, 32-bit NCR SCRIPTS Processor, 32-bit Ethernet controller, two serial ports, eight timers, battery-backed real-time clock
- **MZ 7127** 68340 SBC – 16 MHz 68340 CPU, 1M Flash EPROM, 512K dual-access SRAM, battery-backed real-time clock, four serial ports, 24 programmable I/O channels, SCSI interface (**MZ 7128** includes two M Module slots)
- **MZ 7600** Digital I/O, TTL Compatible – 16 optically isolated inputs and 16 optically isolated outputs (**MZ 7601** for 24/48 Volt operation)
- **MZ 7602** Digital In – 32 optically isolated inputs at 24 or 48 Volts
- **MZ 7603** Digital Out – 32 optically isolated outputs at 24 or 48 Volts
- **MZ 7622** Analog I/O – eight differential or 16 single-ended optically isolated input channels with 12-bit A/D converter, four differential optically isolated output channels (**MZ 7620** for input only, **MZ 7621** for output only)
- **MZ 3000** Live Replacement Capability (LRC) System Unit – Replace modules without interrupting power, includes VMEbus interface, modules available for digital and analog input and output

- **MZ 7640** Motional Control Controller – for up to four closed-loop DC servo drive actuators
- **MZ 7740** High-Resolution Graphics Controller – TI TMS34020 graphics processor, up to 4M video RAM, up to 4M DRAM, resolution up to 1280 × 1024 with 256 colors, standard PC keyboard and mouse interface
- **MZ 7715** Single Board Image Processor – input multiplexer for up to four cameras, A/D conversion to 256 gray levels, input and output lookup tales, two 16×16 correlators and TMS34020 graphics processor
- **MZ 7770** Quad TMS340C40 DSP Board – four TI TMS340C40 graphics processors, each with six communications ports and multichannel DMA
- **MZ 7310** Intelligent Serial Controller – six serial ports
- **MV 7595** High Performance Parallel Interface (HIPPI) – 25 MHz R3051 RISC controller for high-speed point-to-point HIPPI communications, 4M DRAM, up to 512K EPROM, 8K EEPROM, six timers, FIFO message passing

CALL OR WRITE
Mizar, Inc.
2410 Luna Road
Carrollton, Texas 75006
Phone: (214) 277-4600
Fax: (214) 277-4666

User Accounting System from NAS

Native American Services Inc. (Huntsville, Alabama) has released a **User Accounting System** for OS-9. The package can be used by managers and users to track resource utilization on OS-9 systems. The package features on-line queries regarding connections and CPU usage, an option to record logins and session information to disk, and a task profile utility.

CALL OR WRITE
NAS Inc.
3411 Triana Boulevard
Huntsville, Alabama 35805
Phone: (205) 539-7926
Fax: (205) 539-5935

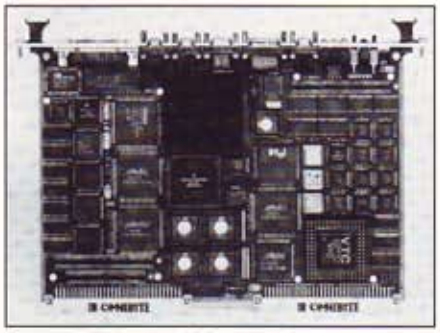
Four New Boards from Omnibyte

Omnibyte Corporation (West Chicago, Illinois) introduced four new boards recently. The **Taurus** is a 6U VMEbus single board computer featuring a 25 MHz 68040 CPU and 25 MHz 68EC030 I/O coprocessor. The board also includes up to 4M DRAM, 128K SRAM, six serial ports, 32 parallel lines, Centronics port, mailbox, watchdog timer, battery-backed calendar clock and up to 8K NVRAM.

Omnibyte's **Jupiter** is a 6U VMEbus multiprotocol communications board that features a 25 MHz 68020 CPU and up to three 68302 microcontrollers. Each 68302 can support one T1 or ISDN channel, or three X.25, HDLC, SDLC, BISYNC, DDCMP, SS7 or V.110 ports.

The **Comet** is a 6U VMEbus analog digitizer board capable of digitizing each of four channels at up to 5 MHz per channel. The board includes up to four digitizer-memory channels, programmable trigger and digitizer clock logic, and VMEbus interface.

The **Aries** SBC features a 25 MHz 68030 primary CPU, secondary 68EC030 CPU, 4M DRAM, 128K SRAM, six serial ports, 32 lines of parallel I/O, Centronics port, six linkable 16-bit times, mailbox, watchdog timer, battery-backed calendar clock and 8K NVRAM. The secondary CPU has two user-selectable modes. In the first mode, the secondary CPU acts as an intelligent I/O processor. In the second mode, the CPU serves as a 32-bit DMA controller, with the primary CPU controlling all I/O devices and I/O interrupts.



The Taurus SBC from Omnibyte.

CALL OR WRITE
Larry Snow, Sales Manager
Omnibyte Corporation
245 West Roosevelt Road
West Chicago, Illinois 60185
Phone: (708) 231-6880

OS-9 Users Group

The **OS-9 Users Group** is a non-profit organization dedicated to excellence in OS-9 computing. A yearly membership fee includes a subscription to the bimonthly journal *MOTD*, a complimentary disk of OS-9 utilities, price discounts from a growing list of OS-9 vendors, and access to the *OS-9 Users Group Software Library*.

OS-9 USERS GROUP
"DEDICATED TO EXCELLENCE IN OS-9 COMPUTING"

CALL OR WRITE
OS-9 Users Group
P.O. Box 71131
Des Moines, Iowa 50325

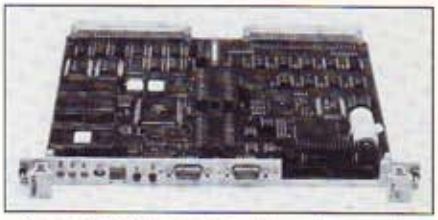
OS-9/X Windows Port for Graphics Processor

Peritek Corporation (Oakland, California) recently announced a single VMEbus graphics board with a port of OS-9/X Windows. The board offers up to 24-bit color with resolution up to 1280 × 1024 pixels from the TI TMS 4020 graphics system processor. Also included is graphics overlay, up to 8M each of display and processor memory, four serial ports, SCSI port, 34082 FPCP socket, hardware pan, zoom and scroll, and Brooktree cursor and color map controllers.

CALL OR WRITE
Peritek Corporation
5550 Redwood Road
Oakland, California 94619
Phone: (510) 531-6500
Fax: (510) 530-8563

Philips' 68340 SBC

Philips Automation Systems (Eindhoven, The Netherlands) recently released their **PG2030/20** single board computer. The 6U VMEbus PG2030/20 features a 16 MHz 68340 CPU, 1M Flash PROM, 512K dual-ported SRAM, two serial ports, serial interface, 24 parallel lines, time-of-day clock, four timer/counters and two DMA channels.



Philips' 68340-based single board computer.

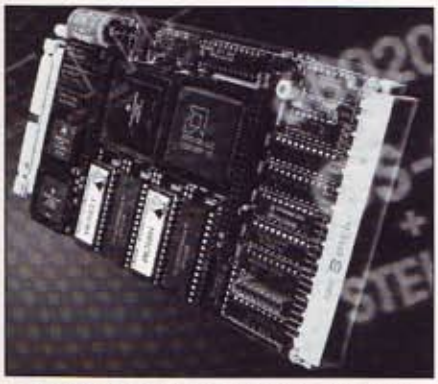
CALL OR WRITE
Eelco van der Wal
VMEbus Business Development
Philips Automation Systems
Building TQ V-3, PO Box 218
5600 MD Eindhoven
The Netherlands
Phone: (31) 40 786167
Fax: (31) 40 786256

STEbus SBC from Pro-Active Control

The **CeleSTE 020** from Pro-Active Control (Cambridge, England) is a 3U STEbus single board computer built around the 68EC020 CPU running at 16 or 25 MHz.

The CeleSTE 020 features up to 1M battery-backed RAM, 2M EPROM, watchdog,

real-time clock/calendar, two fully-configurable serial ports and 20 lines of digital I/O with counters. Plug-in Option Boards can be added for EPROM, disk controllers, FPCP and digital I/O.

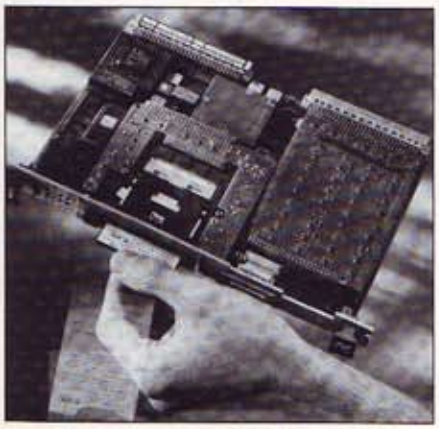


The STEbus CeleSTE 020 from Pro-Active.

CALL OR WRITE
Sue Wallis, Commercial Director
Pro-Active Control
Turing House, Mercers Row
Cambridge CB5 8HY
England
Phone: (44) 223 300801
Fax: (44) 223 300979

PCMCIA Card from Radstone

The 6U VMEbus **APEX-120** expansion interface from Radstone Technology PLC (Towcester, England) uses PCMCIA-compatible memory cards. The APEX-120 is compliant with the PCMCIA Release 2.0 standard and provides up to 64M of programmable EPROM, SRAM or Flash EPROM. The interfaces can be used with any Radstone board that supports the 32-bit APEX expansion bus.



The APEX-120 expansion interface.

CALL OR WRITE
David Compston, Marketing Manager
Radstone Technology PLC
Water Lane
Towcester, Northants NN12 7JN
England
Phone: (44) 327 359444
Fax: (44) 327 359662

Ethernet Boards Supported by Internet Support Package

Rockwell International's CMC Network Products (Santa Barbara, California) announced the availability of their **CMC-130** Ethernet controller. Drivers for the CMC-130, as well as their ENP-10 and ENP-100 products are included in Microware's Internet Support Package.

The CMC-130 features a 9.8M/sec. Ethernet transfer rate and a 36M/sec. VMEbus data transfer rate. The controller is built around a 20 MHz 68020 CPU with 256K DRAM dedicated to the CPU, 256K dual-ported VRAM, software-programmable DMA controller, choice of master or slave operation, and Rockwell's Full Throughput (FXP) architecture.

CALL OR WRITE
Daphne Page
Rockwell International
CMC Network Products
125 Cremona Drive
Santa Barbara, California 93117-5503
Phone: 1-800-CMC-8023 (U.S. Only)
(805) 562-3104
Fax: (805) 968-6478

Graphics Package from SPECTRALAB

SPECTRALAB (Kilchberg, Switzerland) recently announced new versions of two graphics display and plotting packages. Version 1.3 of the **MGR** window manager runs as an overlay of a video frame grabber or as a virtual screen with up to 256 colors and resolution of 2048 × 1024 pixels.

Version 2.8 of SPECTRALAB's **fplot** is a technical and scientific plotting package that drives vector- and bitmap-oriented screens, plotter and printers. fplot also allows for the transfer of vector files.

CALL OR WRITE
Bruno Fricker
SPECTRALAB
Brunnenmoosstraße 7
CH-8802 Kilchberg
Switzerland
Phone: (41) 1 715 38 07
Fax: (41) 1 715 54 47

Two New Products from Syntel

Syntel Microsystems (Huddersfield, England) recently announced the release of **EGOS7**, a graphics tool for use under OS-9. The ***Draw*** utility under EGOS7 is mouse driven and includes pull-down menus, integral editing features, picture segmentation, halftone support and the ability to import TIF format files.

EGOS7 from Syntel Microsystems.

Syntel's **SYN-RXAD8** is an A/D conversion module for VME, G-64 and PCbus boards. The module provides eight individually isolated channels and a 16-bit Delta-Sigma A/D converter. Each input channel can be configured independently for analog input (0 to 10V or +/-10V), or a 4 to 20mA current loop.

CALL OR WRITE
Paul Wilson
Syntel Microsystems
Queens Mill Road
Huddersfield, HD1 3PG
England
Phone: (44) 484 535101
Fax: (44) 484 519363

Text Editor, Formatter Available for OS-9/680X0

Bob van der Poel Software (Wynndel, Canada) recently announced the availability of the **VED** text editor and **VPRINT** formatter for OS-9/680X0. VED features include insert and overstrike modes, automatic indenting, automatic numbering, word wrapping, search, find and replace, and a set of "undo" functions. VPRINT includes support for up to 36 printer fonts, including proportional fonts and extended character sets. Features include multiple column output, and automatic index and table of contents generation.

CALL OR WRITE
Bob van der Poel Software
P.O. Box 57
Wynndel, British Columbia V0B 2N0
Canada
Phone: (604) 868-5772

New Addresses

Two firms announced new addresses:

CALL OR WRITE
American Eltec, Inc.
4340 Stevens Creek Boulevard, Suite 204
San Jose, California 95129
Phone: (408) 244-4700
Fax: (408) 244-5544

CALL OR WRITE
Lloyd I/O, Inc.
P.O. Box 30945
Portland, Oregon 97230
Phone: (503) 222-0702

New Training Seminar Offered

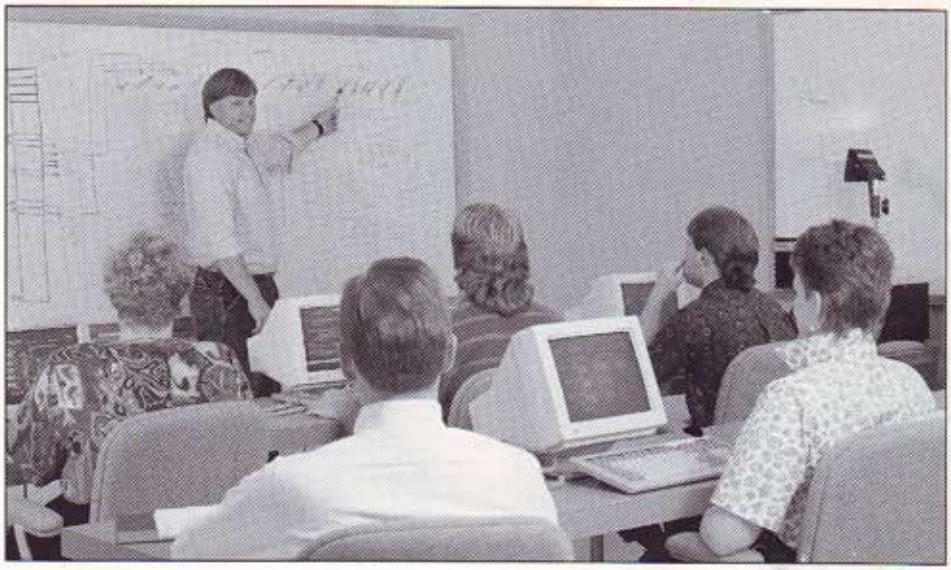
Microware's Training and Education department recently added a new seminar to help developers go far beyond the basics. The **OS-9 Internals Seminar** is geared toward programmers who have extensive knowledge of the OS-9 Real-Time Operating System and want to study the underlying theories and data structures of OS-9.

The OS-9 Internals Seminar includes in-depth examinations of important OS-9 data structures and how different system calls manipulate these structures, the use of system state threads, and the installation of user-written system calls and file managers.

Free OS-9 Insights

The material in the OS-9 Internals Seminar builds upon the second edition of Peter Dibble's *OS-9 Insights: An Advanced Programmer's Guide*. Every attendee at OS-9 Internals Seminars will receive a free copy of the book.

To sign up for Training and Education sessions or for more information, please call Microware's Kristin Doane at (515) 224-1929. Outside the U.S. and Canada, contact your authorized Microware representative. MSC



U.S. Training & Education Winter 1993 Schedule

JANUARY 18-22
OS-9 Starter/Intermediate/Advanced
Oxnard, California

FEBRUARY 1-5
OS-9 Starter/Intermediate/Advanced
Des Moines, Iowa

FEBRUARY 8-12
OS-9 Internals, Networking and Drivers
Des Moines, Iowa

FEBRUARY 16-19
OS-9 Internals and Drivers
Santa Clara, California

FEBRUARY 22-26
OS-9 Starter/Intermediate/Advanced
Boston, Massachusetts

MARCH 2-4
Intermediate/Advanced CD-RTOS
Des Moines, Iowa

MARCH 8-12
OS-9 Starter/Intermediate/Advanced
Melbourne, Florida

MARCH 15-19
OS-9000 Starter/Intermediate/Advanced
Des Moines, Iowa

MARCH 22-23
RAVE
Des Moines, Iowa

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