SYNERTEK
A SUBSIDIARY OF HONEYWELL

Floppy Disk Controller (FDC)

SY6591/SY6591A

MICROPROCESSOR PRODUCTS

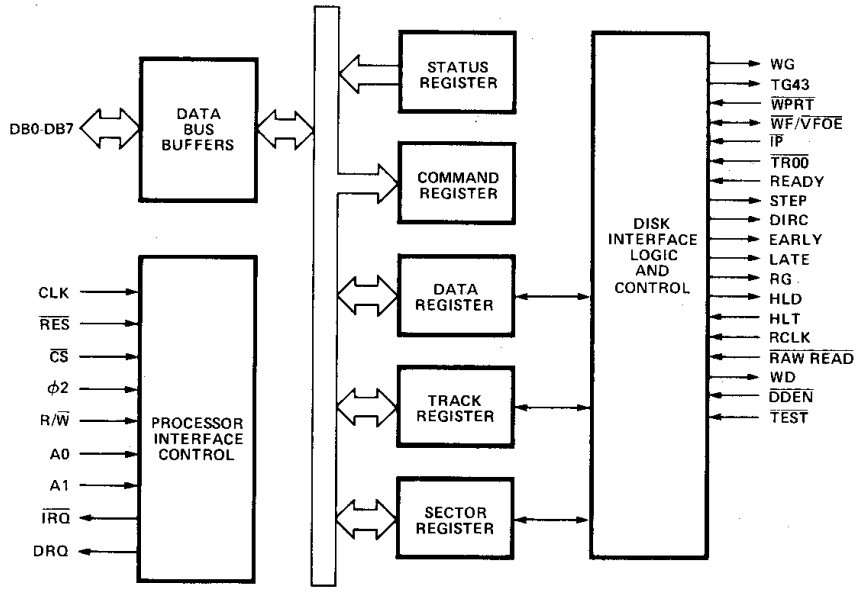
PRELIMINARY

- Functionally compatible with SY1791-02/SY1793-02
- MPU bus interface directly compatible with SY6500 and MC6800 microprocessors.
- Single 5 volt power supply
- Accommodates both single-density (FM) and double-density (MFM) formats
- IBM format compatibility:
  - IBM 3740 Single-Density
  - IBM System-34 Double-Density

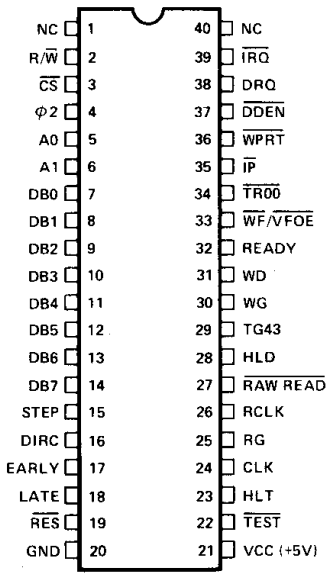
The SY6591 Floppy Disk Controller is a fully programmable device intended for SY6500 or MC6800 microprocessor-based systems. Floppy disk control functions are fully autonomous and are thoroughly described in the SY1791-02/SY1793-02 data sheet. The SY6591 version is different only in the MPU bus interface characteristics.

MICRO PROCESSORS

BLOCK DIAGRAM



PIN ASSIGNMENTS



ORDERING INFORMATION

Part Number	Package	MPU Clock Rate
SYC6591	Ceramic	1MHz
SYD6591	Cerdip	1MHz
SYP6591	Plastic	1MHz
SYC6591A	Ceramic	2MHz
SYD6591A	Cerdip	2MHz
SYP6591A	Plastic	2MHz

DETAILED LIST OF FEATURES

- Single 5 volt (±5%) power supply
- 40-pin package
- Automatic track seek with verification
- Accommodates single-density (FM) and double-density (MFM) formats
- Soft-sector format compatibility
- IBM 3740 (single-density) and System-34 (double-density) compatible
- Single or multiple record read with automatic sector search or entire track read
- Selectable record length (128, 256, 512 or 1024 bytes)
- Single or multiple record write with automatic sector search
- Entire track write for initialization
- Programmable controls:
  - Selectable track-to-track stepping time
  - Selectable head settling and engage times
  - Head position verification
  - Side verification
- Double-buffered read and write data flow
- DMA or programmed data transfers
- TTL-compatible inputs and outputs
- Write precompensation (FM and MFM)
- Comprehensive status register

PROCESSOR INTERFACE SIGNALS

- $\phi 2$ ($\phi 2$) — The $\phi 2$ signal is combined with $\overline{CS}$ to gate the processor interface signals A0, A1 and R/$\overline{W}$ into the floppy disk controller (FDC).
- DATA BUS (DB0-DB7) — This 8-bit non-inverting bidirectional data bus is used for transferring data, control, and status words. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.
- READ/WRITE (R/$\overline{W}$) — This input signal is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read data supplied by the FDC. A low on the R/$\overline{W}$ pin allows data to be written to the FDC.
- INTERRUPT REQUEST ($\overline{IRQ}$) — The $\overline{IRQ}$ is an open drain output. This signal goes low at the completion or termination of any operation and is reset when a new command is loaded into the command register or when the status register is read. An external pull-up resistor to V_{CC} is required when using the SY6591 with a SY6500 or a MC6800 MPU.
- RESET ($\overline{RES}$) — This signal is identical to $\overline{MR}$ on the SY1791-02/SY1793-02. A low on this input resets the device and loads hex 03 into the command register. The Not Ready status bit (status bit 7) is reset during $\overline{RES}$ low. When $\overline{RES}$ is driven high, a Restore command is executed regardless of the state of the Ready signal, and hex 01 is loaded into the Sector Register.
- REGISTER ADDRESS LINES (A0-A1) — These inputs address the internal registers for access by the Data Bus lines under R/$\overline{W}$ and $\phi 2$ control.

REGISTER ADDRESS CODES

A1	A0	READ	WRITE
0	0	STATUS	COMMAND
0	1	TRACK	
1	0	SECTOR	
1	1	DATA	

- READ/WRITE (R/$\overline{W}$) — If $\overline{CS}$ is low, a high on this input enables the addressed internal register to output data onto the data bus when $\phi 2$ is high. If $\overline{CS}$ is low, then a low on this input gates data from the data bus into the addressed register when $\phi 2$ is high.
- CHIP SELECT ($\overline{CS}$) — A low level on this input selects the FDC and enables processor communications with the FDC.
- DATA REQUEST (DRQ) — DRQ is an open drain output. DRQ high during read operations indicates that the Data Register (DR) contains data. When high during write operations, DRQ indicates that the DR is empty and ready to be loaded. DRQ is reset by reading or loading the DR during read or write operations, respectively. Use 10K pull-up resistor to V_{CC}.
- CLOCK (CLK) — This input requires a square wave clock for internal timing reference (2 MHz for 8-inch drives, 1 MHz for 5-inch drives).

FLOPPY DISK CONTROL FUNCTIONS

These functions are identical to those of the SY1791-02/SY1793-02, and are fully described in the corresponding data sheet.

D.C. CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0-70°C) PRELIMINARY

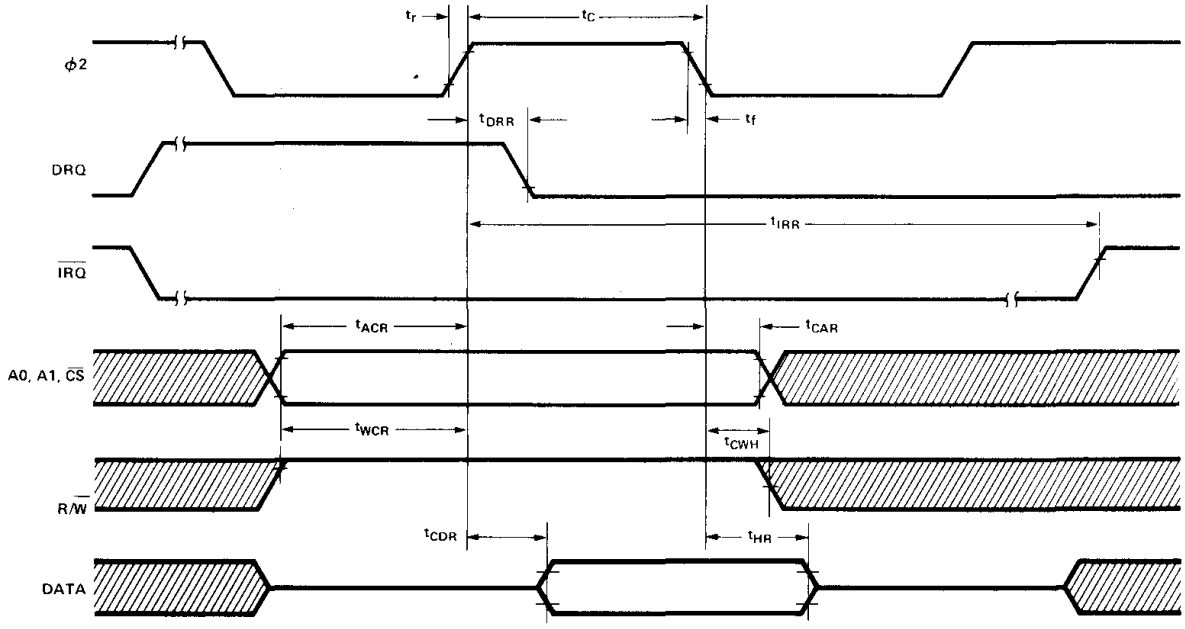
CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage	V_{IH}	2.0	–	V
Input Low Voltage	V_{IL}	–	0.8	V
Input Leakage Current, V_{IN} = 0V to V_{CC}	I_{IL}	–	± 10	μA
Output High Voltage, I_{LOAD} = -100 μA	V_{OH}	2.4	–	V
Output Low Voltage, I_{LOAD} = 1.6 mA	V_{OL}	–	0.4	V
Output Leakage Current, V_{OUT} = V_{CC}	I_{OL}	–	10	μA
Power Dissipation (V_{CC} = 5.25 V)	P_D	–	525	mW
Input Capacitance	C_{IN}	–	15	pF

READ CYCLE (V_{CC} = 5.0V ±5%, T_A = 0 to70°C, unless otherwise noted)

Characteristic	Symbol	6591		6591A		Units
		Min.	Max.	Min.	Max.	
$\phi 2$ Pulse Width	t_C	470	–	235	–	ns
DRQ Reset From $\phi 2$	t_{DRR}	–	500	–	500	ns
$\overline{IRQ}$ Reset From $\phi 2$	t_{IRR}	–	3	–	3	μs
Address Setup Time	t_{ACR}	180	–	90	–	ns
Address Hold Time	t_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Setup Time	t_{WCR}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Access Time	t_{CDR}	–	395	–	200	ns
Data Bus Hold Time	t_{HR}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

READ TIMING



WRITE CYCLE (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	6591		6591A		Units
		Min.	Max.	Min.	Max.	
$\phi 2$ Pulse Width	t_C	470	–	235	–	ns
DRQ Reset From $\phi 2$	t_{DRR}	–	500	–	500	ns
$\overline{IRQ}$ Reset From $\phi 2$	t_{IRR}	–	3	–	3	μs
Address Setup Time	t_{ACW}	180	–	90	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Setup Time	t_{WCW}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Setup Time	t_{DCW}	300	–	150	–	ns
Data Bus Hold Time	t_{HW}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

WRITE TIMING