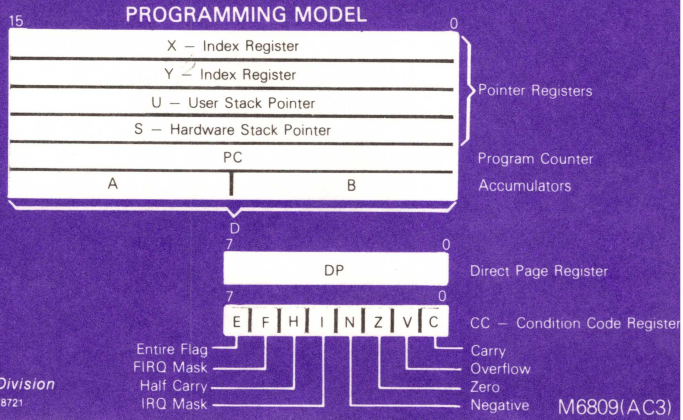


MC6809 — MC6809E

8-bit microprocessor Reference Card



MOTOROLA INC.
MOS Integrated Circuits Division
3501 ED BLUESTEIN BLVD. AUSTIN, TEXAS 78721

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
00	NEG	DIRECT	6	2	1C	ANDCC	IMMED	3	2	2E	BGT	RELATIVE	3	2
03	COM	↑	6	2	1D	SEX	INHERENT	2	1	2F	BLE	RELATIVE	3	2
04	LSR	↑	6	2	1E	EXG	IMMED	8	2	30	LEAX	INDEXED	4	2
06	ROR	↑	6	2	1F	TFR	IMMED	6	2	31	LEAY	↑	4	2
07	ASR	↑	6	2	20	BRA	RELATIVE	3	2	32	LEAS	↕	4	2
08	ASL/LSL	↑	6	2	21	BRN	↑	3	2	33	LEAU	INDEXED	4	2
09	ROL	↑	6	2	22	BHI	↑	3	2	34	PSHS	IMMED	5	2
0A	DEC	↑	6	2	23	BLS	↑	3	2	35	PULS	↑	5	2
0C	INC	↑	6	2	24	BHS/BCC	↑	3	2	36	PSHU	↕	5	2
0D	TST	↑	6	2	25	BLO/BCS	↑	3	2	37	PULU	IMMED	5	2
0E	JMP	↓	3	2	26	BNE	↑	3	2	39	RTS	INHERENT	5	1
0F	CLR	DIRECT	6	2	27	BEQ	↑	3	2	3A	ABX	↑	3	1
12	NOP	INHERENT	2	1	28	BVC	↑	3	2	3B	RTI	INHERENT	6/15	1
13	SYNC	INHERENT	4	1	29	BVS	↑	3	2	3C	CWAI	IMMED	20	2
16	LBRA	RELATIVE	5	3	2A	BPL	↑	3	2	3D	MUL	INHERENT	11	1
17	LBSR	RELATIVE	9	3	2B	BMI	↑	3	2	3F	SWI	↑	19	1
19	DAA	INHERENT	2	1	2C	BGE	↑	3	2	40	NEGA	↕	2	1
1A	ORCC	IMMED	3	2	2D	BLT	RELATIVE	3	2	43	COMA	INHERENT	2	1

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
44	LSRA	INHERENT	2	1	5D	TSTB	INHERENT	2	1	77	ASR	EXTENDED	7	3
46	RORA	↑	2	1	5F	CLRB	INHERENT	2	1	78	ASL/LSL	↑	7	3
47	ASRA	↑	2	1	60	NEG	INDEXED	6	2	79	ROL	↑	7	3
48	ASLA/LSLA	↑	2	1	63	COM	↑	6	2	7A	DEC	↑	7	3
49	ROLA	↑	2	1	64	LSR	↑	6	2	7C	INC	↑	7	3
4A	DECA	↑	2	1	66	ROR	↑	6	2	7D	TST	↑	7	3
4C	INCA	↑	2	1	67	ASR	↑	6	2	7E	JMP	↑	4	3
4D	TSTA	↑	2	1	68	ASL/LSL	↑	6	2	7F	CLR	EXTENDED	7	3
4F	CLRA	↑	2	1	69	ROL	↑	6	2	80	SUBA	IMMED	2	2
50	NEGB	↑	2	1	6A	DEC	↑	6	2	81	CMPA	↑	2	2
53	COMB	↑	2	1	6C	INC	↑	6	2	82	SBCA	↑	2	2
54	LSRB	↑	2	1	6D	TST	↑	6	2	83	SUBD	↑	4	3
56	RORB	↑	2	1	6E	JMP	↑	3	2	84	ANDA	↑	2	2
57	ASRB	↑	2	1	6F	CLR	INDEXED	6	2	85	BITA	↑	2	2
58	ASLB/LSLB	↑	2	1	70	NEG	EXTENDED	7	3	86	LDA	↑	2	2
59	ROLB	↑	2	1	73	COM	↑	7	3	88	EORA	↑	2	2
5A	DECB	↑	2	1	74	LSR	↑	7	3	89	ADCA	↑	2	2
5C	INCB	INHERENT	2	1	76	ROR	EXTENDED	7	3	8A	ORA	↑	2	2

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
8B	ADDA	IMMED	2	2	9E	LDX	DIRECT	5	2	B0	SUBA	EXTENDED	5	3
8C	CMPX	IMMED	4	3	9F	STX	DIRECT	5	2	B1	CMPA	↑	5	3
8D	BSR	RELATIVE	7	2	A0	SUBA	INDEXED	4	2	B2	SBCA	↑	5	3
8E	LDX	IMMED	3	3	A1	CMPA	↑	4	2	B3	SUBD	↑	7	3
90	SUBA	DIRECT	4	2	A2	SBCA	↑	4	2	B4	ANDA	↑	5	3
91	CMPA	↑	4	2	A3	SUBD	↑	6	2	B5	BITA	↑	5	3
92	SBCA	↑	4	2	A4	ANDA	↑	4	2	B6	LDA	↑	5	3
93	SUBD	↑	6	2	A5	BITA	↑	4	2	B7	STA	↑	5	3
94	ANDA	↑	4	2	A6	LDA	↑	4	2	B8	EORA	↑	5	3
95	BITA	↑	4	2	A7	STA	↑	4	2	B9	ADCA	↑	5	3
96	LDA	↑	4	2	A8	EORA	↑	4	2	BA	ORA	↑	5	3
97	STA	↑	4	2	A9	ADCA	↑	4	2	BB	ADDA	↑	5	3
98	EORA	↑	4	2	AA	ORA	↑	4	2	BC	CMPX	↑	7	3
99	ADCA	↑	4	2	AB	ADDA	↑	4	2	BD	JSR	↑	8	3
9A	ORA	↑	4	2	AC	CMPX	↑	6	2	BE	LDX	↓	6	3
9B	ADDA	↑	4	2	AD	JSR	↑	7	2	BF	STX	EXTENDED	6	3
9C	CMPX	↓	6	2	AE	LDX	↑	5	2	C0	SUBB	IMMED	2	2
9D	JSR	DIRECT	7	2	AF	STX	INDEXED	5	2	C1	CMPB	IMMED	2	2

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
C2	SBCB	IMMED	2	2	D7	STB	DIRECT	4	2	E9	ADCB	INDEXED	4	2
C3	ADDD		4	3	D8	EORB		4	2	EA	ORB		4	2
C4	ANDB		2	2	D9	ADCB		4	2	EB	ADDB		4	2
C5	BITB		2	2	DA	ORB		4	2	EC	LDD		5	2
C6	LDB		2	2	DB	ADDB		4	2	ED	STD		5	2
C8	EORB		2	2	DC	LDD		5	2	EE	LDU		5	2
C9	ADCB		2	2	DD	STD		5	2	EF	STU	INDEXED	5	2
CA	ORB		2	2	DE	LDU		5	2	F0	SUBB	EXTENDED	5	3
CB	ADDB		2	2	DF	STU	DIRECT	5	2	F1	CMPB		5	3
CC	LDD		3	3	E0	SUBB	INDEXED	4	2	F2	SBCB		5	3
CE	LDU	IMMED	3	3	E1	CMPB		4	2	F3	ADDD		7	3
D0	SUBB	DIRECT	4	2	E2	SBCB		4	2	F4	ANDB		5	3
D1	CMPB		4	2	E3	ADDD		6	2	F5	BITB		5	3
D2	SBCB		4	2	E4	ANDB		4	2	F6	LDB		5	3
D3	ADDD		6	2	E5	BITB		4	2	F7	STB		5	3
D4	ANDB		4	2	E6	LDB		4	2	F8	EORB		5	3
D5	BITB		4	2	E7	STB		4	2	F9	ADCB		5	3
D6	LDB	DIRECT	4	2	E8	EORB	INDEXED	4	2	FA	ORB	EXTENDED	5	3

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
FB	ADDB	EXTENDED	5	3	102E	LBGT	RELATIVE	5(6)	4	10CE	LDS	IMMED	4	4
FC	LDD		6	3	102F	LBLE	RELATIVE	5(6)	4	10DE	LDS	DIRECT	6	3
FD	STD		6	3	103F	SWI2	INHERENT	20	2	10DF	STS	DIRECT	6	3
FE	LDU		6	3	1083	CMPD	IMMED	5	4	10EE	LDS	INDEXED	6	3
FF	STU	EXTENDED	6	3	108C	CMPY		5	4	10EF	STS	INDEXED	6	3
1021	LBRN	RELATIVE	5	4	108E	LDY	IMMED	4	4	10FE	LDS	EXTENDED	7	4
1022	LBHI		5(6)	4	1093	CMPD	DIRECT	7	3	10FF	STS	EXTENDED	7	4
1023	LBLS		5(6)	4	109C	CMPY		7	3	113F	SWI3	INHERENT	20	2
1024	LBHS/LBCC		5(6)	4	109E	LDY		6	3	1183	CMPU	IMMED	5	4
1025	LBGS/LBLO		5(6)	4	109F	STY	DIRECT	6	3	118C	CMPS	IMMED	5	4
1026	LBNE		5(6)	4	10A3	CMPD	INDEXED	7	3	1193	CMPU	DIRECT	7	3
1027	LBEQ		5(6)	4	10AC	CMPY		7	3	119C	CMPS	DIRECT	7	3
1028	LBVC		5(6)	4	10AE	LDY		6	3	11A3	CMPU	INDEXED	7	3
1029	LBVS		5(6)	4	10AF	STY	INDEXED	6	3	11AC	CMPS	INDEXED	7	3
102A	LBPL		5(6)	4	10B3	CMPD	EXTENDED	8	4	11B3	CMPU	EXTENDED	8	4
102B	LBMI		5(6)	4	10BC	CMPY		8	4	11BC	CMPS	EXTENDED	8	4
102C	LBGE		5(6)	4	10BE	LDY		7	4					
102D	LBLT	RELATIVE	5(6)	4	10BF	STY	EXTENDED	7	4					

STACKING ORDER

Pull Order

- ↓
- CC
- A
- B
- DP
- X Hi
- X Lo
- Y Hi
- Y Lo
- U/S Hi
- U/S Lo
- PC Hi
- PC Lo

↑

Increasing Memory

INTERRUPT VECTORS

- FFFF Restart
- FFFC NMI
- FFFA SWI
- FFF8 IRQ
- FFF6 FIRQ
- FFF4 SWI2
- FFF2 SWI3
- FFF0 Reserved

MC6809

VSS	1	40	HALT
NMI	2	39	XTAL
IRQ	3	38	EXTAL
FIRQ	4	37	RESET
BS	5	36	MRDY
BA	6	35	Q
VCC	7	34	E
A0	8	33	DMA/BREQ
A1	9	32	R/W
A2	10	31	D0
A3	11	30	D1
A4	12	29	D2
A5	13	28	D3
A6	14	27	D4
A7	15	26	D5
A8	16	25	D6
A9	17	24	D7
A10	18	23	A15
A11	19	22	A14
A12	20	21	A13

MC6809E

VSS	1	40	HALT
NMI	2	39	TSC
IRQ	3	38	LIC
FIRQ	4	37	RESET
BS	5	36	AVMA
BA	6	35	Q
VCC	7	34	E
A0	8	33	BUSY
A1	9	32	R/W
A2	10	31	D0
A3	11	30	D1
A4	12	29	D2
A5	13	28	D3
A6	14	27	D4
A7	15	26	D5
A8	16	25	D6
A9	17	24	D7
A10	18	23	A15
A11	19	22	A14
A12	20	21	A13

HEXADEXIMAL AND DECIMAL CONVERSION

HOW TO USE THE TABLES

CONVERSION TO DECIMAL: Find the decimal weights for corresponding hexadecimal characters beginning with the least significant character. The sum of the decimal weight is the decimal value of the hexadecimal number.

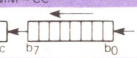
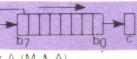
CONVERSION TO HEXADEXIMAL: Find the highest decimal value in the table which is lower than or equal to the decimal number to be converted. The corresponding hexadecimal character is the most significant character. Subtract the decimal value found from the decimal number to be converted. With the difference, repeat the process to find subsequent hexadecimal characters.

HEXADEXIMAL AND DECIMAL CONVERSION								
15	BYTE	8	7	BYTE	0			
15	CHAR	12	11	CHAR	8	7	CHAR	0
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	DEC
0	0	0	0	0	0	0	0	0
1	4	096	1	256	1	16	1	1
2	8	192	2	512	2	32	2	2
3	12	288	3	768	3	48	3	3
4	16	384	4	1024	4	64	4	4
5	20	480	5	1280	5	80	5	5
6	24	576	6	1536	6	96	6	6
7	28	672	7	1792	7	112	7	7
8	32	768	8	2048	8	128	8	8
9	36	864	9	2304	9	144	9	9
A	40	960	A	2560	A	160	A	10
B	45	1056	B	2816	B	176	B	11
C	49	1152	C	3072	C	192	C	12
D	53	1248	D	3328	D	208	D	13
E	57	1344	E	3584	E	224	E	14
F	61	1440	F	3840	F	240	F	15


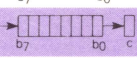

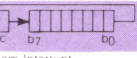
ASCII CHARACTER SET

Most Significant Character								
Hex	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	-	p
1	SOH	DC1	1	A	Q	a	q	
2	STX	DC2	2	B	R	b	r	
3	ETX	DC3	3	C	S	c	s	
4	EOT	DC4	4	D	T	d	t	
5	ENQ	NAK	5	E	U	e	u	
6	ACK	SYN	6	F	V	f	v	
7	BEL	ETB	7	G	W	g	w	
8	BS	CAN	8	H	X	h	x	
9	HT	EM	9	I	Y	i	y	
A	LF	SUB		J	Z	j	z	
B	VT	ESC		K	[k	[
C	FF	FS	<	L	\	l	\	
D	CR	GS	=	M]	m]	
E	SO	RS	>	N	^	n	^	
F	SI	US	?	O	_	o	_	DEL

POWERS OF TWO			
2 ⁿ	n	2 ⁿ	n
1	0	128	7
2	1	256	8
4	2	512	9
8	3	1,024	10
16	4	2,048	11
32	5	4,096	12
64	6	8,192	13
			14
			15
			16
			17
			18
			19
			20

Instruction	Forms	Addressing Modes									Description	H N Z V C												
		Immediate			Direct			Indexed ¹				Extended			Inherent			H	N	Z	V	C		
		Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#					
ABX														3A	3	1	B + X - X (Unsigned)	*	*	*	*	*		
ADC	ADCA ADCB	89 2 2 C9 2 2	2 2	99 4 2 D9 4 2	2 2	A9 4+ 2+ E9 4+ 2+	2 2	B9 5 3 F9 5 3	5 3								A + M + C - A B + M + C - B	1	1	1	1	1		
ADD	ADDA ADDB ADDD	8B 2 2 CB 2 2 C3 4 3	2 2	9B 4 2 DB 4 2 D3 6 2	2 2	AB 4+ 2+ EB 4+ 2+ E3 6+ 2+	2 2	BB 5 3 FB 5 3 F3 7 3	5 3								A + M - A B + M - B D + M + M + 1 - D	1	1	1	1	1		
AND	ANDA ANDB ANDCC	84 2 2 C4 2 2 1C 3 2	2 2	94 4 2 D4 4 2	2 2	A4 4+ 2+ E4 4+ 2+	2 2	B4 5 3 F4 5 3	5 3								A & M - A B & M - B CC & IMM - CC	*	1	1	0	*		
ASL	ASLA ASLB ASL			08 6 2	2	68 6+ 2+	2	78 7 3		48 2 1 58 2 1								7	1	1	1	1		
ASR	ASRA ASRB ASR			07 6 2	2	67 6+ 2+	2	77 7 3		47 2 1 57 2 1								7	1	1	1	1		
BIT	BITA BITB	85 2 2 C5 2 2	2 2	95 4 2 D5 4 2	2 2	A5 4+ 2+ E5 4+ 2+	2 2	B5 5 3 F5 5 3	5 3								Bit Test: A (M, A, A) Bit Test: B (M, A, B)	*	1	1	0	*		
CLR	CLRA CLRB CLR			0F 6 2	2	6F 6+ 2+	2	7F 7 3		4F 2 1 5F 2 1							0 - A 0 - B 0 - M	*	0	1	0	0		
CMP	CMPA CMPB CMPD	81 2 2 C1 2 2 10 5 4	2 2	91 4 2 D1 4 2 10 7 3	2 2	A1 4+ 2+ E1 4+ 2+ A3 7+ 3+	2 2	B1 5 3 F1 5 3 B3 10 8 4	5 3								Compare M from A Compare M from B Compare M M + 1 from D	7	1	1	1	1		
	CMPS	11 5 4	4	11 7 3	3	11 7+ 3+	3	11 8 4	4								Compare M M + 1 from S	*	1	1	1	1		
	CMPL	11 5 4	4	11 7 3	3	11 7+ 3+	3	11 8 4	4								Compare M M + 1 from U	*	1	1	1	1		
	CMPX CMPY	8C 4 3 10 5 4 8C	3 3	9C 6 2 10 7 3 9C	2 2	AC 6+ 2+ 10 7+ 3+	2 2	BC 7 3 10 8 4 BC	7 3								Compare M M + 1 from X Compare M M + 1 from Y	*	1	1	1	1		

Instruction	Forms	Addressing Modes									Description	H N Z V C												
		Immediate			Direct			Indexed ¹				Extended			Inherent			H	N	Z	V	C		
		Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#					
COM	COMA COMB COM					03 6 2	2	63 6+ 2+	2	73 7 3				43 2 1 53 2 1				A - A B - B M - M	*	1	1	0	1	
CWAI		3C	≥20	2														CC & IMM - CC Wait for Interrupt					7	
DAA														19 2 1				Decimal Adjust A	*	1	1	0	1	
DEC	DECA DECB DEC					0A 6 2	2	6A 6+ 2+	2	7A 7 3				4A 2 1 5A 2 1				A - 1 - A B - 1 - B M - 1 - M	*	1	1	1	*	
EOR	EORA EORB	88 2 2 C8 2 2	2 2	98 4 2 D8 4 2	2 2	A8 4+ 2+ E8 4+ 2+	2 2	B8 5 3 F8 5 3	5 3								A ⊕ M - A B ⊕ M - B	*	1	1	0	*		
EXG	R1, R2	1E	8	2													R1 - R2 ²	*	*	*	*	*		
INC	INCA INCB INC					0C 6 2	2	6C 6+ 2+	2	7C 7 3				4C 2 1 5C 2 1				A + 1 - A B + 1 - B M + 1 - M	*	1	1	1	*	
JMP						0E 3 2	2	6E 3+ 2+	2	7E 4 3							EA ³ - PC	*	*	*	*	*		
JSR						9D 7 2	2	AD 7+ 2+	2	BD 8 3								Jump to Subroutine	*	*	*	*	*	
LD	LDA LDB LDD LDS	86 2 2 C6 2 2 CC 3 3 10 4 4	2 2	96 4 2 D6 4 2 DC 5 2 10 6 3	2 2	A6 4+ 2+ E6 4+ 2+ EC 5+ 2+ 10 6+ 3+	2 2	B6 5 3 F6 5 3 FC 6 3 10 7 4	5 3									M - A M - B M M + 1 - D M M + 1 - S	*	1	1	0	*	
	LDU LDX LDY	CE 3 3 8E 3 3 10 4 4	3 3	DE 5 2 9E 5 2 10 6 3	2 2	EE 5+ 2+ AE 5+ 2+ 10 6+ 3+	2 2	FE 6 3 BE 6 3 10 7 4	6 3								M M + 1 - U M M + 1 - X M M + 1 - Y	*	1	1	0	*		
LEA	LEAS LEAU LEAX LEAY					32 4+ 2+ 33 4+ 2+ 30 4+ 2+ 31 4+ 2+	2 2										EA ³ - S EA ³ - U EA ³ - X EA ³ - Y	*	*	*	*	*		

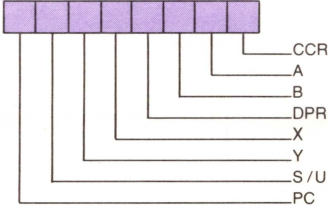
Instruction	Forms	Addressing Modes									Description	H N Z V C												
		Immediate			Direct			Indexed ¹				Extended			Inherent			H	N	Z	V	C		
		Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#					
LSL	LSLA LSLB LSL					08 6 2	2	68 6+ 2+	2	78 7 3				48 2 1 58 2 1					*	1	1	1	1	
LSR	LSRA LSRB LSR					04 6 2	2	64 6+ 2+	2	74 7 3				44 2 1 54 2 1					*	0	1	*	1	
MUL														3D 11 1				A × B -> D (Unsigned)	*	*	*	*	8	
NEG	NEGA NEGB NEG					00 6 2	2	60 6+ 2+	2	70 7 3				40 2 1 50 2 1				A - 1 - A B - 1 - B M - 1 - M	7	1	1	1	1	
NOF														12 2 1				No Operation	*	*	*	*	*	
OR	ORA ORB ORCC	8A 2 2 CA 2 2 1A 3 2	2 2	9A 4 2 DA 4 2	2 2	AA 4+ 2+ EA 4+ 2+	2 2	BA 5 3 FA 5 3	5 3									A V M - A B V M - B CC V IMM - CC	*	1	1	0	*	
PSH	PSHS PSHU	34 5+ 4 36 5+ 4	2 2															Push Registers on S Stack Push Registers on U Stack	*	*	*	*	*	
PUL	PULS PULU	35 5+ 4 37 5+ 4	2 2															Pull Registers from S Stack Pull Registers from U Stack	*	*	*	*	*	
ROL	ROLA ROLB ROL					09 6 2	2	69 6+ 2+	2	79 7 3				49 2 1 59 2 1					*	1	1	1	1	
ROR	RORA RORB ROR					06 6 2	2	66 6+ 2+	2	76 7 3				46 2 1 56 2 1					*	1	1	1	1	
RTI														3B 6/15 1				Return From Interrupt	*	*	*	*	6	
RTS														39 5 1				Return from Subroutine	*	*	*	*	*	
SBC	SBCA SBCB	82 2 2 C2 2 2	2 2	92 4 2 D2 4 2	2 2	A2 4+ 2+ E2 4+ 2+	2 2	B2 5 3 F2 5 3	5 3								A - M - C - A B - M - C - B	8	1	1	1	1		
SEX														1D 2 1				Sign Extend B into A	*	1	1	0	*	

Instruction	Forms	Addressing Modes									Description	H N Z V C												
		Immediate			Direct			Indexed ¹				Extended			Inherent			H	N	Z	V	C		
		Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#					
ST	STA STB STD STS					97 4 2 D7 4 2 DD 5 2 10 6 3	2 2	A7 4+ 2+ E7 4+ 2+ ED 5+ 2+ 10 6+ 3+	2 2	B7 5 3 F7 5 3 FD 6 3 10 7 4	5 3								A - M B - M D - M M + 1 S - M M + 1	*	1	1	0	*
	STU STX STY					DF 5 2 9F 5 2 10 6 3 9F	2 2	EF 5+ 2+ AF 5+ 2+ 10 6+ 3+ AF 6+ 3+	2 2	FF 6 3 BF 6 3 10 7 4 BF	6 3								U - M M + 1 X - M M + 1 Y - M M + 1	*	1	1	0	*
SUB	SUBA SUBB SUBD	80 2 2 C0 2 2 83 4 3	2 2	90 4 2 D0 4 2 93 6 2	2 2	A0 4+ 2+ E0 4+ 2+ A3 6+ 2+	2 2	B0 5 3 F0 5 3 B3 7 3	5 3									A - M - A B - M - B D - M M + 1 - D	7	1	1	1	1	
SWI	SWI ⁵ SWI ²⁵ SWI ³⁵													3F 19 1 20 2 2 3F 11 20 1 3F				Software Interrupt 1 Software Interrupt 2 Software Interrupt 3	*	*	*	*	*	
SYNC														13 ≥4 1				Synchronize to Interrupt	*	*	*	*	*	
TFR	R1, R2	1F	6	2														R1 - R2 ²	*	*	*	*	*	
TST	TSTA TSTB TST					0D 6 2	2	6D 6+ 2+	2	7D 7 3				4D 2 1 5D 2 1				Test A Test B Test M	*	1	1	0	*	

Legend:
 OP Operation Code (Hexadecimal)
 ~ Number of MPU Cycles
 # Number of Program Bytes
 + Arithmetic Plus
 M Complement of M
 - Transfer Into
 H Half-carry (from bit 3)
 N Negative (sign bit)
 Z Zero Result
 V Overflow (Carry-out)
 I Test and set if true, cleared otherwise
 * Not Affected
 CC Condition Code Register
 : Concatenation
 V Logical or
 A Logical and

- Notes:
- This column gives a base cycle and byte count. To obtain total count, add the values obtained from the INDEXED ADDRESSING MODES table.
 - R1 and R2 may be any pair of 8 bit or any pair of 16 bit registers.
The 8 bit registers are: A, B, CC, DP
The 16 bit registers are: X, Y, U, S, D, PC
 - EA is the effective address.
 - The PSH and PUL instructions require 5 cycles plus 1 cycle for each byte pushed or pulled.
 - SWI sets I and F bits. SWI2 and SWI3 do not affect I and F.
 - Conditions Codes set as a direct result of the instruction.
 - Value of half-carry flag is undefined.
 - Special Case — Carry set if b7 is SET.

PUSH/PULL POST BYTE



TRANSFER/EXCHANGE POST BYTE



REGISTER FIELD (Source or Destination)

- | | |
|----------------|------------|
| 0000 = D (A:B) | 0101 = PC |
| 0001 = X | 1000 = A |
| 0010 = Y | 1001 = B |
| 0011 = U | 1010 = CCR |
| 0100 = S | 1011 = DPR |

INDEXED ADDRESSING MODES

Type	Forms	Non Indirect			Indirect		
		Assembler Form	Postbyte OP Code	x + #	Assembler Form	Postbyte OP Code	+ #
Constant Offset From R (two's complement offset)	No Offset	.R	1RR00100	0 0	[R]	1RR10100	3 0
	5 Bit Offset	n. R	0RRnnnnn	1 0	defaults to 8-bit		
	8 Bit Offset	n. R	1RR01000	1 1	[n. R]	1RR11000	4 1
	16 Bit Offset	n. R	1RR01001	4 2	[n. R]	1RR11001	7 2
Accumulator Offset From R (two's complement offset)	A — Register Offset	A. R	1RR00110	1 0	[A. R]	1RR10110	4 0
	B — Register Offset	B. R	1RR00101	1 0	[B. R]	1RR10101	4 0
	D — Register Offset	D. R	1RR01011	4 0	[D. R]	1RR11011	7 0
Auto Increment/Decrement R	Increment By 1	.R+	1RR00000	2 0	not allowed		
	Increment By 2	.R++	1RR00001	3 0	[R++]	1RR10001	6 0
	Decrement By 1	.R-	1RR00010	2 0	not allowed		
	Decrement By 2	.R--	1RR00011	3 0	[--R]	1RR10011	6 0
Constant Offset From PC (two's complement offset)	8 Bit Offset	n. PCR	1XX01100	1 1	[n. PCR]	1XX11100	4 1
	16 Bit Offset	n. PCR	1XX01101	5 2	[n. PCR]	1XX11101	8 2
Extended Indirect	16 Bit Address	—	—	— --	[n]	10011111	5 2

R = X, Y, U or S X = 00 Y = 01
 X = Don't Care U = 10 S = 11

+ and + Indicate the number of additional cycles and bytes for the particular variation

BRANCH INSTRUCTIONS

Instruction	Forms	Addressing Mode		Description	Conditions												
		OP	#		5	3	2	1	0	H	N	Z	V	C			
BCC	BCC	24	3	2	Branch C = 0	*	*	*	*	*	*	*	*	*	*	*	*
	LBCC	10	5(6)	4	Long Branch C = 0	*	*	*	*	*	*	*	*	*	*	*	*
BCS	BCS	25	3	2	Branch C = 1	*	*	*	*	*	*	*	*	*	*	*	*
	LBCS	10	5(6)	4	Long Branch C = 1	*	*	*	*	*	*	*	*	*	*	*	*
BEQ	BEQ	27	3	2	Branch Z = 1	*	*	*	*	*	*	*	*	*	*	*	*
	LBEQ	10	5(6)	4	Long Branch Z = 1	*	*	*	*	*	*	*	*	*	*	*	*
BGE	BGE	2C	3	2	Branch <= Zero	*	*	*	*	*	*	*	*	*	*	*	*
	LBGE	10	5(6)	4	Long Branch <= Zero	*	*	*	*	*	*	*	*	*	*	*	*
BGT	BGT	2E	3	2	Branch > Zero	*	*	*	*	*	*	*	*	*	*	*	*
	LBGT	10	5(6)	4	Long Branch > Zero	*	*	*	*	*	*	*	*	*	*	*	*
BHI	BHI	22	3	2	Branch Higher	*	*	*	*	*	*	*	*	*	*	*	*
	LBHI	10	5(6)	4	Long Branch Higher	*	*	*	*	*	*	*	*	*	*	*	*
BHS	BHS	24	3	2	Branch Higher or Same	*	*	*	*	*	*	*	*	*	*	*	*
	LBHS	10	5(6)	4	Long Branch Higher or Same	*	*	*	*	*	*	*	*	*	*	*	*
BLE	BLE	2F	3	2	Branch <= Zero	*	*	*	*	*	*	*	*	*	*	*	*
	LBLE	10	5(6)	4	Long Branch <= Zero	*	*	*	*	*	*	*	*	*	*	*	*
BLO	BLO	25	3	2	Branch lower	*	*	*	*	*	*	*	*	*	*	*	*
	LBLO	10	5(6)	4	Long Branch Lower	*	*	*	*	*	*	*	*	*	*	*	*

Instruction	Forms	Addressing Mode		Description	Conditions												
		OP	#		5	3	2	1	0	H	N	Z	V	C			
BLS	BLS	23	3	2	Branch Lower	*	*	*	*	*	*	*	*	*	*	*	*
	LBLS	10	5(6)	4	Long Branch Lower or Same	*	*	*	*	*	*	*	*	*	*	*	*
BLT	BLT	2D	3	2	Branch < Zero	*	*	*	*	*	*	*	*	*	*	*	*
	LBLT	10	5(6)	4	Long Branch < Zero	*	*	*	*	*	*	*	*	*	*	*	*
BMI	BMI	2B	3	2	Branch Minus	*	*	*	*	*	*	*	*	*	*	*	*
	LBMI	10	5(6)	4	Long Branch Minus	*	*	*	*	*	*	*	*	*	*	*	*
BNE	BNE	26	3	2	Branch Z = 0	*	*	*	*	*	*	*	*	*	*	*	*
	LBNE	10	5(6)	4	Long Branch Z = 0	*	*	*	*	*	*	*	*	*	*	*	*
BPL	BPL	2A	2	2	Branch Plus	*	*	*	*	*	*	*	*	*	*	*	*
	LBPL	10	5(6)	4	Long Branch Plus	*	*	*	*	*	*	*	*	*	*	*	*
BRA	BRA	20	3	2	Branch Always	*	*	*	*	*	*	*	*	*	*	*	*
	LBRA	16	5	3	Long Branch Always	*	*	*	*	*	*	*	*	*	*	*	*
BRN	BRN	21	3	2	Branch Never	*	*	*	*	*	*	*	*	*	*	*	*
	LB RN	10	5	4	Long Branch Never	*	*	*	*	*	*	*	*	*	*	*	*
BSR	BSR	BD	7	2	Branch to Subroutine	*	*	*	*	*	*	*	*	*	*	*	*
	LB SR	17	9	3	Long Branch to Subroutine	*	*	*	*	*	*	*	*	*	*	*	*
BVC	BVC	28	3	2	Branch V = 0	*	*	*	*	*	*	*	*	*	*	*	*
	LBVC	10	5(6)	4	Long Branch V = 0	*	*	*	*	*	*	*	*	*	*	*	*
BVS	BVS	29	3	2	Branch V = 1	*	*	*	*	*	*	*	*	*	*	*	*
	LBVS	10	5(6)	4	Long Branch V = 1	*	*	*	*	*	*	*	*	*	*	*	*

SIMPLE BRANCHES

	OP	#	#
BRA	20	3	2
LBRA	16	5	3
BRN	21	3	2
LB RN	1021	5	4
BSR	8D	7	2
LB SR	17	9	3

SIMPLE CONDITIONAL BRANCHES (NOTES 1-4)

Test	True	OP	False	OP
N = 1	BMI	2B	BPL	2A
Z = 1	BEQ	27	BNE	26
V = 1	BVS	29	BVC	28
C = 1	BCS	25	BCC	24

SIGNED CONDITIONAL BRANCHES (NOTES 1-4)

Test	True	OP	False	OP
r > m	BGT	2E	BLE	2F
r ≥ m	BGE	2C	BLT	2D
r = m	BEQ	27	BNE	26
r ≤ m	BLE	2F	BGT	2E
r < m	BLT	2D	BGE	2C

UNSIGNED CONDITIONAL BRANCHES (NOTES 1-4)

Test	True	OP	False	OP
r > m	BHI	22	BLS	23
r ≥ m	BHS	24	BLO	25
r = m	BEQ	27	BNE	26
r ≤ m	BLS	23	BHI	22
r < m	BLO	25	BHS	24

- Notes:
- All conditional branches have both short and long variations.
 - All short branches are 2 bytes and require 3 cycles.
 - All conditional long branches are formed by prefixing the short branch opcode with \$10 and using a 16-bit destination offset.
 - All conditional long branches require 4 bytes and 6 cycles if the branch is taken or 5 cycles if the branch is not taken.